*Meeting The New Oscillator Jitter Characterization*

## VCXO Fulfills SONET "Offset Jitter" Specs (1ps RMS @ 12 kHz - 20 MHz)

**Advanced datacom applications require VCXO jitter to be specified at frequencies outside the cleanup range of phase locked loop data recovery circuits. Phase locked loops typically reject jitter to 12 kHz, requiring components with tight "offset jitter" specifications beyond 12 kHz. Series M2912 VCXOs specifiy 1 ps maximum "offset jitter" from 12 kHz to 20 MHz. The oscillators also meet the linearity requirements of advanced phase locked loop applications, provide guaranteed capture specs, feature excellent frequency stability, and develop differential output for noise immunity.**

### Stringent New Jitter Specification

Series M2912 VCXOs are ultra low jitter voltage controlled crystal oscillators based on differential PECL logic and which unequivocally guarantee ±50 ppm, ±75 ppm or ±100 ppm capture (pull) for all rated operating conditions. In particular, these VCXOs meet the new and especially stringent SONET jitter specification referred to as offset jitter. Series M2912 are exceptional VCXOs and this release highlights their advanced features. The release also attempts to provide insight into the new *offset jitter* specification.

Rising data rates and customer demands for reliable communications have created the need for the rigorous new VCXO jitter characterization. Offset jitter refers to the range of frequencies outside the correction capabilities of signal conditioning phase locked loops. Series M2912 VCXOs meet the requirements of SONET and other advanced communications systems with maximum offset jitter of 1 ps RMS for the 12 kHz to 20 MHz range.
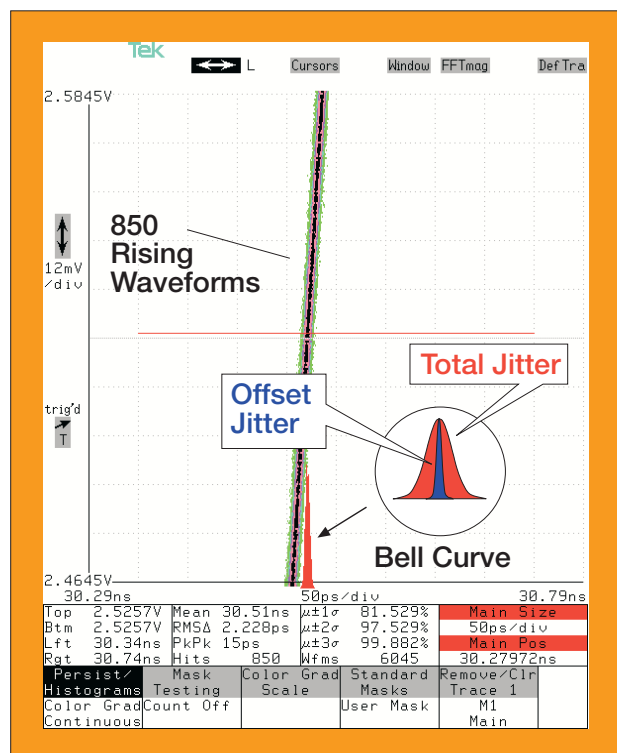


Figure 1—Sampling oscilloscope presents waveform timing (jitter) distribution for 850 leading edge M2912 waveforms. Color changes from black (center) through red, orange, purple, and then green on either side, denote increased timing error. (See also Figure 2). Excellent M2912 jitter performance (total jitter) is displayed by bell curve, which shows very tight distribution of sampled waveforms. Bell curve confirms that most of the jitter is concentrated around the fundamental (carrier)waveform. Figure 4 shows relationship between total jitter and offset jitter.

## Sampling Scope Displays Jitter

For a start, the storage oscilloscope display, Figure 1, presents a composite jitter picture for 850 repetitive signal waveforms. Maximum jitter is expressed by the horizontal width of the composite waveform. Different colors display jitter density. (Shown more clearly in Figure 2).

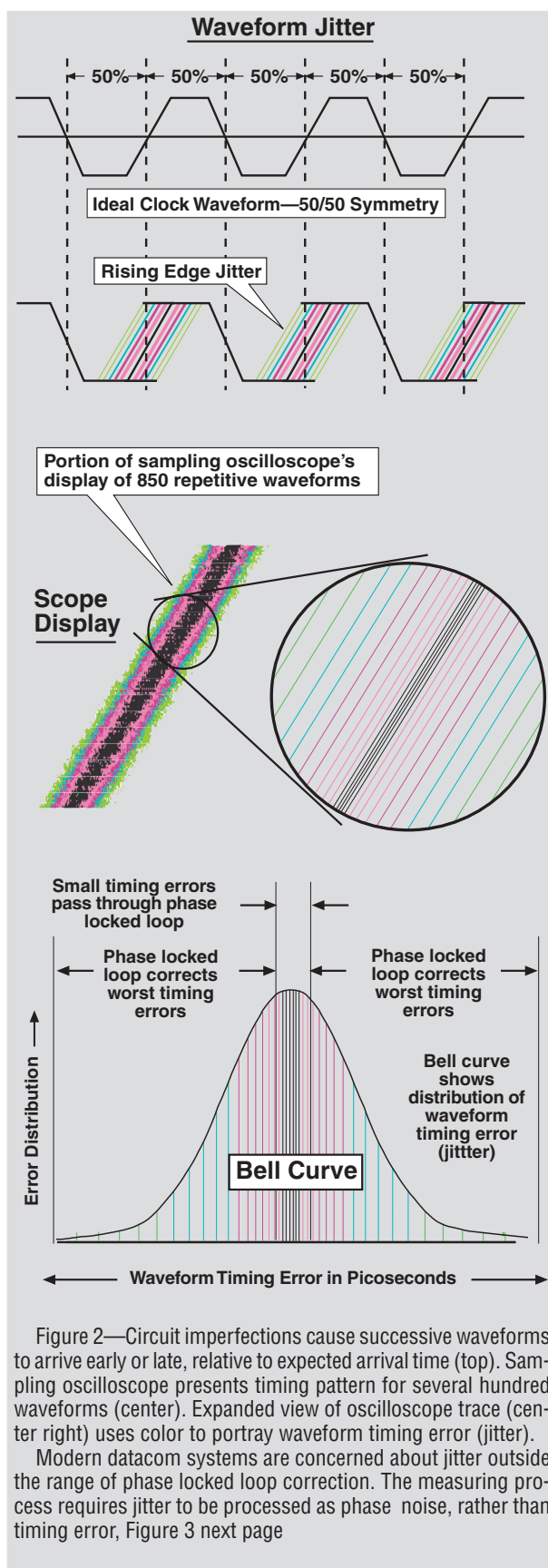## Bell Curve Confirms Tight Jitter Control

Figure 2 is an expanded version of the information behind Figure 1's sampling scope display. Repeated waveforms (Figure 2, top) are advanced or delayed relative to their ideal position in time. Falling edges are also subject to jitter, although not shown in Figure 2.

An expanded section of oscilloscope display (center) shows the distribution of waveform jitter. The jitter pattern shows most timing errors to be concentrated at the minimal displacement value. A proportionately decreasing fraction of the 850 waveforms occupy time slots more distant (in time) from the ideal time.

A bell curve (bottom) presents the distribution of timing error more rigorously. The curve's horizontal axis is divided into time slots, while the vertical axis is divided according to data density. In other words, vertical increments mark off an increasing number of waveforms per slot. For instance, with zero jitter, all 850 waveforms would fit into the single tallest slot. In fact, most of the 850 advanced or delayed waveforms occur within picoseconds of the fundamental. As delay time increases, fewer and fewer waveforms fit within subsequent time slots. Because jitter shown here is a random process, jitter density conforms to the classic Gaussian bell curve distribution.

## Jitter As Phase Noise

Figure 3 introduces the concept of jitter ex-



Figure 2—Circuit imperfections cause successive waveforms to arrive early or late, relative to expected arrival time (top). Sampling oscilloscope presents timing pattern for several hundred waveforms (center). Expanded view of oscilloscope trace (center right) uses color to portray waveform timing error (jitter).

Modern datacom systems are concerned about jitter outside the range of phase locked loop correction. The measuring process requires jitter to be processed as phase noise, rather than timing error, Figure 3 next page

pressed as phase modulation (phase noise) rather than an error in time. The bell curve (Figure 3, top) showing jitter distribution as timing error, could alternatively be viewed as expressing error in phase.

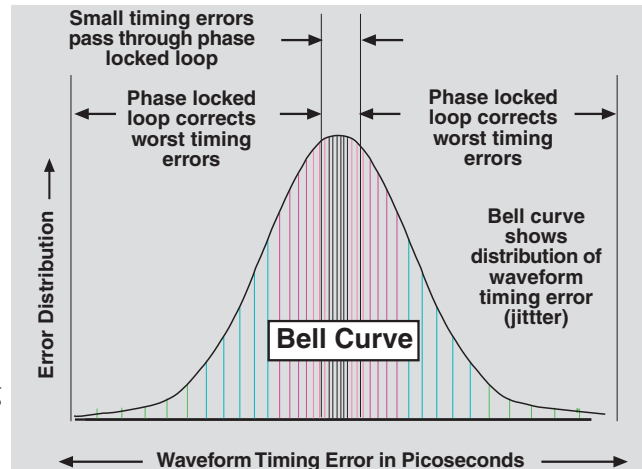## Jitter As Frequency Distribution

Changes in phase imply a modulating effect in the frequency domain. Consequently, it is not too a great stretch to conceive of jitter as being a pattern of noise *frequencies* modulating the signal. In fact, a spectrum analyzer is used to measure frequency spectrum and power in selected frequency "slots", much as a sampling oscilloscope assigns timing error to time slots.

## Spectrum Analysis

Figure 3 starts with jitter as a timing error (bell curve, top), then gives a spectrum analyzer's representation of the same jitter (lower diagram) as a phase noise plot. The larger the timing error, the larger the phase deviation. Because typical jitter is random, and frequency deviation symmetrical about the fundamental, spectrum analyzers need display only positive-going frequencies.
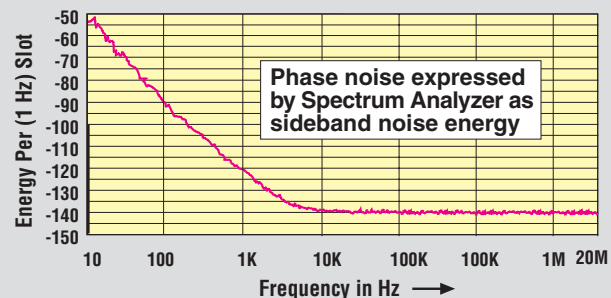
## Frequencies Per 1 Hz Increment

Frequency deviation (bottom), is expressed horizontally. The analyzer's task is analogous to the sampling oscilloscope's. Namely, to determine how the pattern of jitter frequencies is grouped into each successive 1 Hz "slot" of rising frequency. Unlike the sampling oscilloscope, the spectrum analyzer does not compute the *number* of waveforms (frequencies) for each 1 Hz "slot." Instead, the instrument



**Jitter is most easily understood as variations in waveform timing. However, the same jitter can also be viewed as variations in phase— or even frequency.**



**This spectrum analyzer plot expresses jitter in terms of frequencies displaced at 1 Hz increments from the fundamental frequency. Instead of plotting the *number* of frequencies in each 1 Hz "slot", the instrument plots the relative energy in dB. The fewer the frequencies per slot, the lower the energy.**

Figure 3—Bell curve (top) presents the sampling oscilloscope's much enlarged pattern of timing deviation for the 850 repetitive waveforms. In operation, the oscilloscope might divide the horizontal axis into one- picoseconds slots. All 850 wavefom samples would then be allocated to an appropriate slot, in accordance with the extent of it's time error.

The spectrum analyzer operates analogously, creating "slots" one hertz wide. It then allocates the jitters' energy to the appropriate slot, in accordance with its offset frequency.

presents a frequency deviation pattern in terms of decreasing energy. The less the spectral power at a given frequency, the lower the energy in that 1 Hz slot. Frequency energy is expressed vertically, in decreasing dB relative to the fundamental.

## Concentration Around Carrier

Figure 3's spectrum analyzer displays the rapid decrease in energy of the frequency components as their frequency increases. (That is, as frequency differs from the carrier). In fact, the curve is virtually flat beyond about 20 kHz.

## Deriving Offset Frequency

The spectrum analyzer's frequency-based data is key to computing jitter in picoseconds (time) for the SONET offset frequency specification. Figure 4 shows why the value is needed, and how the spectrum analyzer is key to computing the value.

Offset jitter in picoseconds is computed from the area under the curve for the frequency range of interest. For Series M2912, the specification calls for maximum offset jitter between 12 kHz to 20 MHz. There is a direct relationship between jitter represented as phase noise, and jitter in picoseconds RMS values. From the RMS data, peak-to-peak values of offset jitter are readily approximated. For Model M2912, maximum 12 kHz to 20 MHz offset jitter is 1 ps RMS, (Bottom diagram).

## Why 12 kHz - 20 MHz Offset Jitter?

Why do SONET and other advanced datacom applications call for an RMS jitter specification covering 12 kHz to 20 MHz? Why not 0 kHz to 20 MHz.

Reference to Figure 4 helps explain the specification. It arises because datacom systems employ phase locked loop (PLL) signal conditioning circuits to correct for the close-in 0 - 12 kHz jitter. Both bell curve and spectrum analyzer show the highest concentration of jitter within the PLL's coverage. Significantly, the PLL does not correct for jitter beyond this narrow range. To achieve optimal circuit perfor-
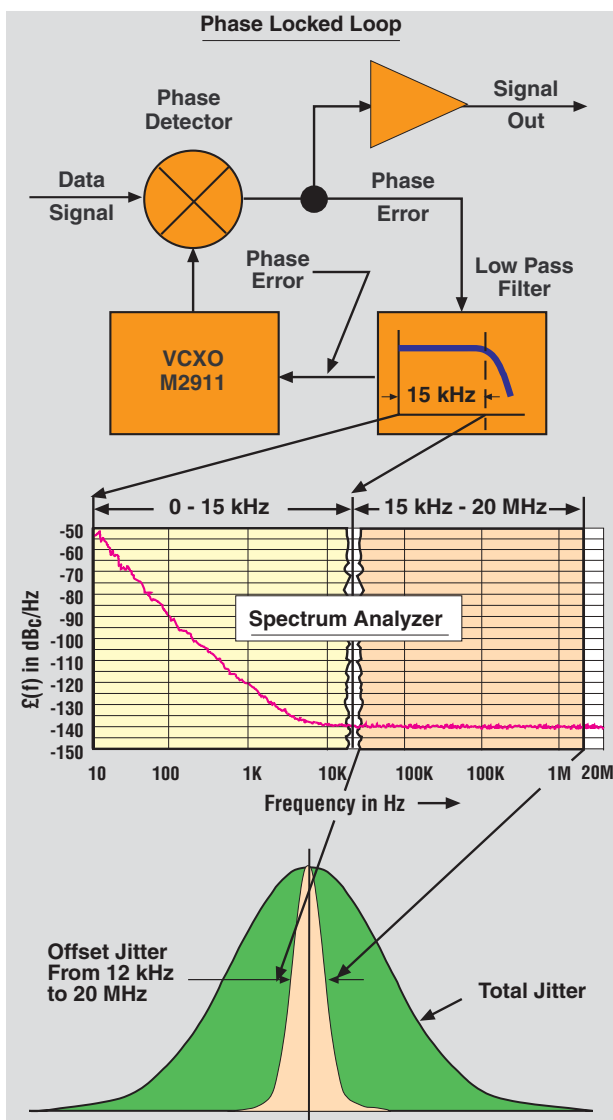


**M2912's 12 kHz to 20 MHz jitter specification is derived from spectrum analyzer's data. The analyzer expresses jitter in terms of frequency components displaced at 1 Hz intervals from fundamental frequency. Jitter of interest is calculated in picoseconds RMS from the area under the orange region of the curve**

Figure 4—Advanced datacom equipment builders extract data signals from jitter and noise using phase locked loop (PLL) techniques (top). Operating on the phase noise, a phase locked loop removes jitter and noise closest to the fundamental frequency. The illustration shows how the PLL's filter defines the range of signal reconditioning—typically DC to 12 kHz. This is the region of maximum jitter, as the bell curve and spectrum analyzer displays demonstrate.

Nonetheless, there's still jitter on the incoming signal at frequencies (or time variations), beyond the PLL's DC - 12 kHz span. Consequently, components used in PLL circuitry are selected to contribute minimal jitter in this "offset frequency" range. Actual offset jitter value is computed from the spectrum analyzer data for the desired frequency range. (12 kHz to 20 MHz for Series M2912).

mance, therefore, equipment builders require circuit components with minimal jitter outside the range of the PLL's compensating capability.

# Electrical, Mechanical And Thermal Specifications

## Specification Overview

MF Electronics' high performance 5-volt Series M2912 ECLPS logic VCXOs guarantee frequency capture values (pull ranges) of ±50 ppm, ±75 ppm and ±100 ppm. The VCXOs are available for 15 MHz to 175 MHz center frequency, provide differential output for noise rejecting signal transmission, and operate over the 0°C to 70°C temperature range. The new VCXOs provide exceptional specifications on all key fronts, including linearity, stability, waveform symmetry, and rise time, The M2912 family features the lowest jitter of all MF Electronics' VCXOs, and additionally, meets the new OFFSET JITTER specification of SONET and other advanced datacom systems. Subsequent paragraphs will describe these specifications in greater detail.

Series M2912 VCXOs meet the 2:1 maximum-to-minimum frequency-voltage slope variation requirements, Figure 5, of advanced phase locked loops. (Referred to as Deviation Sensitivity Ratio). Typical waveform rise and fall times are 225 picoseconds. Fast rise waveforms minimize ambiguity in determining whether a logic value is ONE or ZERO. Waveform symmetry is 48/52, which is very close to the ideal 50/50.
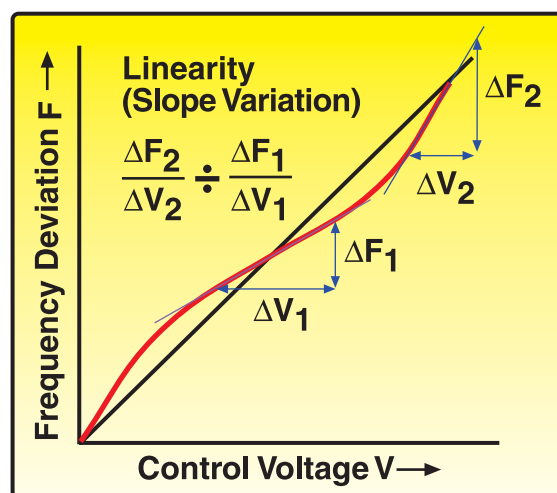


Figure 5—Ideal VCXO frequency-voltage curve is a straight line with constant slope. Actual curve departs from true straight line, introducing variations in the $\Delta F/\Delta V$ slope. (Voltage-frequency control sensitivity). Modern phase locked loop circuits require the ratio between maximum slope and minimum slope (deviation sensitivity ratio) to be less than 2:1. VCXOs in the M2912 family easily meet this requirement.

Series M2912 VCXOs ease the user's system design task with the 0.5V to 4.5V full scale control voltage range. (Instead of requiring the user to provide 0V to 5V frequency control voltage). Pull bandwidth is 10 kHz minimum bandwidth. Center frequency stability is ±20 ppm from 0°C to 70°C. Total M2912 family jitter is 4 ps RMS maximum, 2 -3 ps RMS typical. The stringent OFFSET JITTER specification is 1 ps RMS maximum over the 12 kHz to 20 MHz band. Series M2912 VCXOs operate on 5VDC ± 10% supplies—and sustain normal operation during supply voltage dips to 4.5V. Maximum current draw is 70 mA at 5V.

**Mechanical Data**—Series M2912 VCXOs are manufactured in standard stainless steel 0.5" x 0.8" x 0.2" Size M through hole packages, and are available in conductive tubes for pick-and place manufacturing automation. An internal 0.1 μF bypass capacitor decouples noise from the DC power bus. All oscillators versions are tested at 0°C, 20°C and 70°C.

## Applications

The M2912 VCXO's very low jitter, and frequency to 175 MHz, provide high stability references sources for frequency multiplication to the gigahertz range of gigabit ethernet, ATM, SONET, and other high speed communications systems.

## Contact • Delivery • Price

Low jitter series M2912 VCXOs are manufactured by MF Electronics Corp. 10 Commerce Drive, New Rochelle, NY 10801

**Contact:**    (Sales)
           Tel: (800) 331-1236 • Fax: (914) 712-2290
           email:  sales@mfelectronics.com
           internet: http://www.mfelectronics.com
           (Editorial)— Stan Froud • Tel: (212) 787-0448 • sfroud@nyc.rr.com

**Delivery:**    Stock to 6 weeks.

**Price:**    Below $55 in OEM quantity. (Varies with frequency and capture range)