FEUP Universidade do Porto
Faculdade de Engenharia

Departamento de Engenharia Electrotécnica e de Computadores

Guide to the study of

MULTISTAGE DIFFERENTIAL AMPLIFIERS

Franclim F. Ferreira
Pedro Guedes de Oliveira
Vítor Grade Tavares

March 2004

MULTISTAGE DIFFERENTIAL AMPLIFIERS

INSTRUCTIONS

Read the Instructions to know how you can better use this work. Know how it is organized and which navigation tools are available. See how you can complement the study with the simulation of some of the circuits presented here.

INDEX

See the table of contents of this work. The table is organized through a pop down menu revealed when you place the cursor over the titles. Through the Index you can directly access each one of the sections and exercises of this work.

ANNEXES

The main text of this work is enhanced with several complementary texts, in order to help the reader about matters not directly studied here. These are matters which are supposed to be studied before or later. Through the main text there are several links to these texts but you can also access them through the table of Annexes, organized in a similar way as the main Index.

1. Introduction

Operational amplifiers (OpAmps) with negative feedback allow highly versatile realisations, in particular highly stabilised gain amplifiers. In fact, today's amplifiers are mostly utilised with feedback.

Take the example depicted in fig. 1. This inverting amplifier has a voltage gain, v_o / v_i, very approximately equal to $-R_2 / R_1$. To make this quantity a reasonable approximation it is simply required a very high open loop gain (i.e., $A >> R_2 / R_1$, although it may vary significantly), a high input resistance ($R_i\ A >> R_2$), and a small output resistance ($R_o << R_2$). (*Note: A, R_i and R_o are the OpAmp equivalent model parameters*)

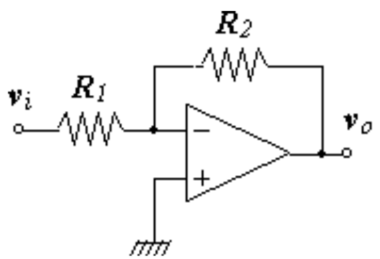


fig. 1 - Inverting montage

Taking the basic BJTs or FETs amplifying configurations as reference, a natural question arises: *How to realise an amplifier to attain such goals (i.e., that shows sufficiently high gain, high input resistance, and small output resistance)?*

From the set of basic single transistor amplifiers, the BJT's common emitter (CE) topology [or FET's common source (CS)] is the configuration that simultaneously allows the highest voltage gain with a R_i not too small.

Thus, the amplifier above could be realised with a single transistor as indicated in fig. 2.

Resistors R_2 and R_1 define the gain. By direct analysis, it can easily be shown that the gain is given by v_o / v_i @ -9,1 (verify it as an exercise), which is reasonably close to $- R_2 / R_1 = - 10$.

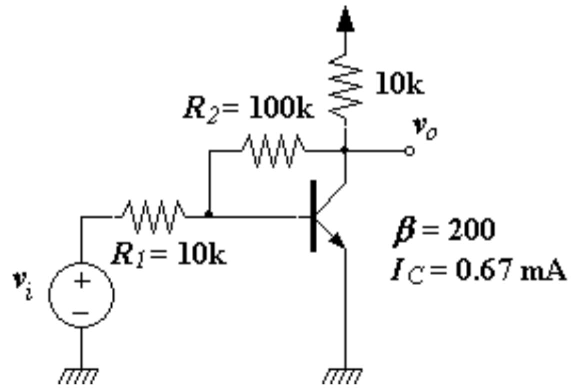


fig. 2 - Common emitter configuration

Nevertheless, it is notorious that the CE configuration, by itself, does not bring together the conditions to a satisfactory OpAmp characteristics.

For example, it does not implement a differential input (consequently, the CE amplifier does not allow the non-inverting implementation), it has a relatively small input resistance and a high output resistance (R_i @ r_p and R_o @ 100 kW // 10 kW).

Inserting a resistor between the emitter terminal and ground will boost the input resistance. Yet, this procedure reduces the gain (and increases the output resistance, although marginally). Alternatively, FETs can be used at the input - at the cost of lower g_m and consequently lower gains. Nonetheless, no juggling will confer a symmetrical differential input to the CE topology.

The solution resorts to a composed implementation (with more than one transistor) to obtain a differential input called the differential pair.

Note, however, that other OpAmp characteristics should be searched for, such as: very high gain, high input and low output resistance, low voltage and current offsets. Simultaneously, one should not loose site for other characteristic improvements, such as band width and maximum slew-rate.

2. Differential pair

Consider fig. 3 setting where a differential pair is implemented with two BJTs.

If, $v_{B1} = v_{B2} = v_{CM}$ (common mode voltage), the voltages v_{C1} and v_{C2} will not change even when v_{CM} varies (within certain limits set by the need to keep the transistors in active mode).

On the other hand, if v_{B1} ¹ v_{B2}, the voltages v_{C1} and v_{C2} will no longer be equal.

Thus, we may say that the differential pair (ideally) responds to differential signals (i.e., the input voltage difference) and rejects the common mode, i.e., does not react to identical signals at both inputs.

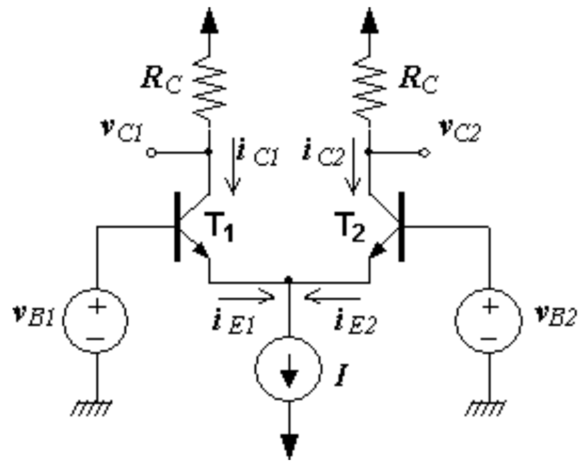


fig. 3 – Bipolar differential pair

2.1. Current variation

2.1.1. BJT

The total emitter current is kept constant by the current source I. Therefore, when the input differential voltage $v_D = v_{B2} - v_{B1}$ changes in time, some of the current of a given transistor will be transferred to the other. This change in transistor current with input differential variation can be observed in fig. 4.

The expression for the current can be found to be:

$$i_{C1,2} = \frac{\alpha I}{1 + e^{\pm v_D / V_T}}$$

The differential pair operation is approximately linear for small differential input voltages. This corresponds to a region in the graph where the exponential exhibits an approximate linear behaviour. In fact, it can be shown that for $v_D = V_T$ @ 25 mV, the gain changes about 20%.

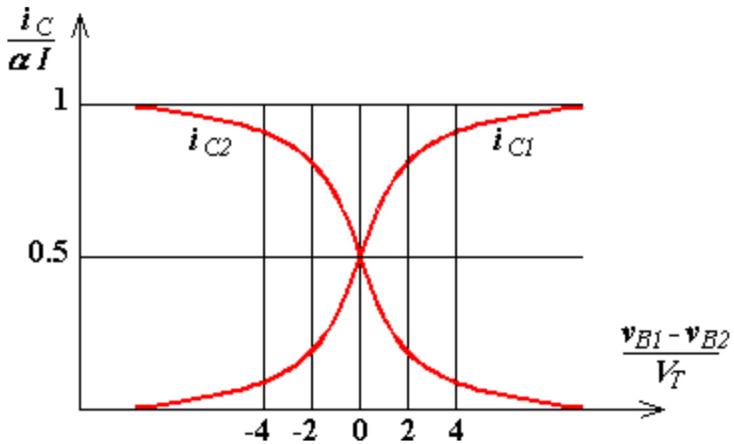


fig. 4 – BJT differential pair currents

On the other hand, a ±100 mV input differential voltage is enough for almost all the current to be drawn by one of the transistors.

2.1.2. FET

The basic schematic is similar to a bipolar differential pair and is shown in fig. 5 (JFET example).

The analysis is very similar to the differential bipolar case. Having in mind that:

$$i_D = I_{DSS}\left(1 - \frac{v_{GS}}{V_P}\right)^2$$

naming $v_{id} = v_{G1} - v_{G2}$

and making $i_{D1} + i_{D2} = I$

we get:

$$i_{D1,2} = \frac{I}{2} \pm v_{id}\frac{I}{-2V_P}\sqrt{2\frac{I_{DSS}}{I} - \left(\frac{v_{id}}{V_P}\right)^2\left(\frac{I_{DSS}}{I}\right)^2}$$

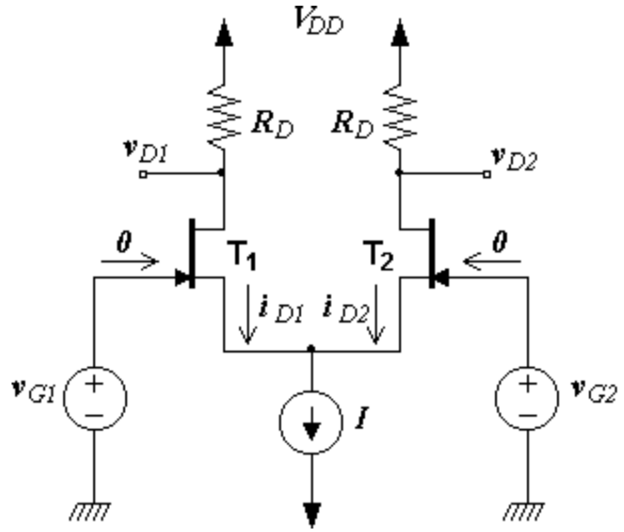


fig. 5 – JFET differential pair

This current changes as a function of v_{id} and is shown in fig. 6. The FET's parameters used in this example is also shown on the graph.

The main remarks, relatively to the bipolar differential pair, are, on one hand, the larger v_{id} value spread, and, on the other hand, the smaller characteristics slope around the origin.

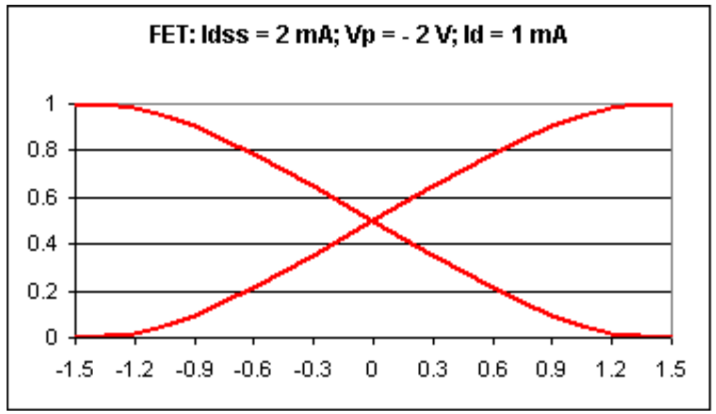


fig. 6 – JFET differential pair currents

The MOSFET differential pair analysis (see fig. 7, where it is shown a MOSFET differential pair with enhancement MOSFETS – channel n) is not only similar to a JFET, but also the same conclusions are driven.

In fact, the MOSFET current function is the same of the JFET, however is commonly written in a different form as:

$$i_D = K(v_{GS} - V_t)^2$$

Consequently, the current versus v_d is the same, however with a different form:

$$i_{D1,2} = \frac{I}{2} \pm \sqrt{2KI}\left(\frac{v_{id}}{2}\right)\sqrt{1 - \frac{(v_{id}/2)^2}{I/2K}}$$

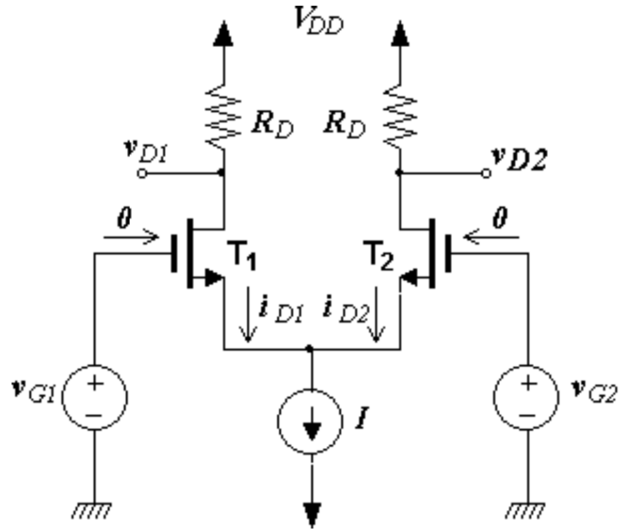


fig. 7 – MOSFET differential pair

2.2. Small signal operation

Take the BJT differential pair as reference. If around $v_D = 0$ we find:

$$\left.\frac{di_C}{dv_D}\right|_{v_D=0} = \frac{i_c}{v_d} \qquad \text{we get} \qquad i_c = \frac{\alpha I}{2V_T}\frac{v_d}{2} = g_m\frac{v_d}{2}$$

An alternative point of view to get the same result is to observe fig. 8 schematic for small signals.

The input differential resistance is $R_{id} = 2\,r_p$, because looking into the base of any transistor we see

$r_p + (1+b)\,r_e = 2r_p$.

Having in mind, for example, that:

$$v_{c1} = -R_C \frac{v_d}{2\, r_\pi} \beta = -R_C \frac{v_d}{2} g_m$$

for the three possible outputs the following differential gains result:

$$A_{d1} = \frac{v_{c1}}{v_d} = -\frac{1}{2} g_m R_C$$

$$A_{d2} = \frac{v_{c2}}{v_d} = \frac{1}{2} g_m R_C$$

$$A_{dd} = \frac{v_{c1} - v_{c2}}{v_d} = -g_m R_C$$

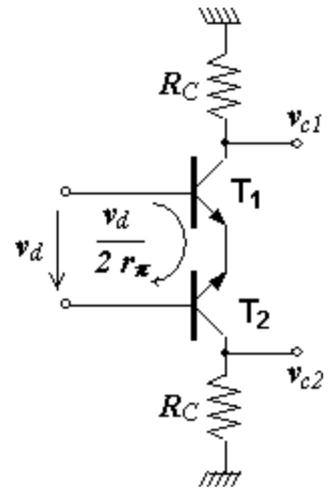


fig. 8 – Small signal operation

This last gain corresponds to an amplifier with differential signals both at the input and output (fig. 9).

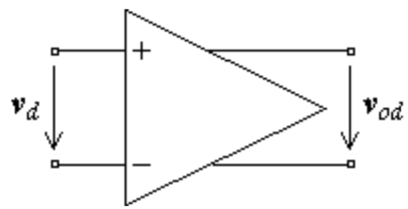
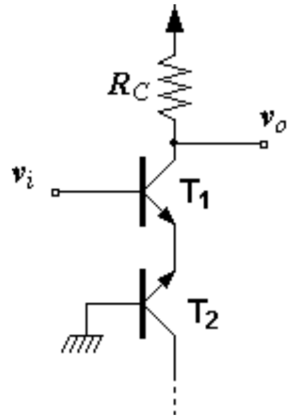


fig. 9 – Differential input and output amplifier

There is another way to look into this problem:

If we consider the amplifier as an ideal differential amplifier (where essentially the common mode gain is null), according to fig. 10 circuit, the response to a signal v_i can be analysed with the base of T_2 connected to ground: The collector of T_2 does not influence T_1. This last transistor is in common emitter configuration with an emitter resistance R_E equal to $r_{e2} = 1/g_{m2}$. Then, the gain is approximately:

$$A = -\frac{R_C}{R_E + 1/g_{m1}} = -\frac{R_C}{1/g_{m2} + 1/g_{m1}} \cong -\frac{g_m R_C}{2}$$



However, if the other output is intended, it is enough to think that both collector currents (signal) are necessarily equal, and, consequently, the gain will be symmetric of the indicated above.

Nonetheless, it is called the attention upon the fact that this configuration corresponds to a variant of a circuit known as *cascode* that it will be studied ahead.

fig. 10 – Alternative method for evaluating the differential pair gain

Exercise 1: *If in fig. 3 schematic, emitter resistors are inserted, as observed in fig. 11, find the gain and the differential input resistance.*

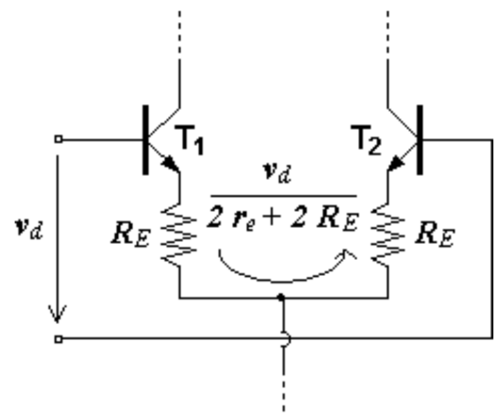


fig. 11 – Differential pair with emitter resistances

Answer

Solution

A small signal analysis can also be done taking the equivalence between the differential pair and the CE configuration.

Even assuming that the biasing source is not ideal (see fig. 12), in rigorous terms and in differential operation, i.e., $v_{B1} = v_d/2$ and $v_{B2} = -v_d/2$, the common node at the emitters can be represented by a virtual ground, where a transistor "gets" a $+v_d/2$ signal and the other a $-v_d/2$. Thus, each transistor is equivalent to a CE configuration with a grounded emitter, as shown in fig. 13.

From fig. 13 we get:

$$\frac{v_{c1}}{v_d/2} = -g_m R_C$$

or, if transistor's r_o cannot be ignored:

$$\frac{v_{c1}}{v_d/2} = -g_m (R_C // r_o)$$

Since $A_{d1} = v_{c1} / v_d$ it results:

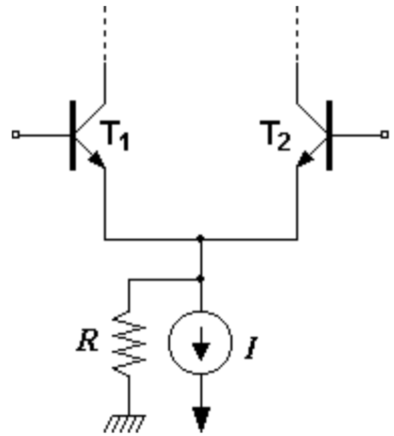


fig. 12 – Non ideal biasing source

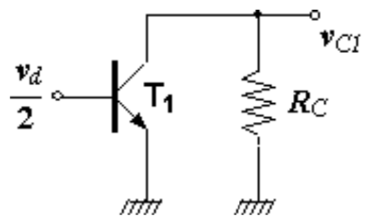


fig. 13 – Equivalent CE montage

$$A_{d1} = -\frac{1}{2} g_m (R_C // r_o)$$ and, naturally, $A_{d2} = -A_{d1}$ e $A_{dd} = 2\ A_{d1}$.

A similar analysis can be performed on a FET differential pair. The sole relevant difference is the linear operation span which is significantly bigger in a FET differential pair. It may reach some volts while a bipolar pair is restricted around ± 25 mV.

Thus, we get:

$$A_{d1} = \frac{v_{d1}}{v_{id}} = -\frac{g_m R_D}{2} \quad , \quad A_{d2} = \frac{v_{d2}}{v_{id}} = \frac{g_m R_D}{2} \quad \text{and} \quad A_{dd} = \frac{v_o}{v_{id}} = -g_m R_D$$

If it is not possible to ignore r_o, we have to change R_D by the parallel $R_D // r_o$.

2.3. Common mode operation

The common mode operation is illustrated in fig. 14.

Due to symmetry and to the equality $v_{B1} = v_{B2}$, half circuit analysis is sufficient, as shown in fig. 15 (*note that, for common mode signals, resistor R can be substituted by two 2R resistors, in parallel, which allows us the analysis of each transistor in separate*).

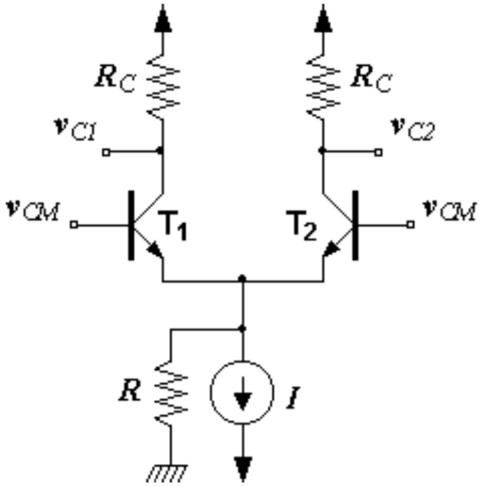


fig. 14 – Common mode operation

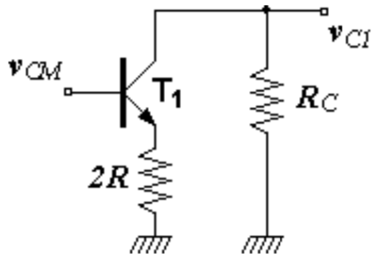


fig. 15 – Common mode equivalent CE montage

If $R_C \ll r_o$, we get:

$$A_{c1} = \frac{v_{c1}}{v_{CM}} = -\frac{\alpha R_C}{r_e + 2R} \cong -\frac{R_C}{2R}$$ and by analogy $$A_{c2} = \frac{v_{c2}}{v_{CM}} \cong -\frac{R_C}{2R}$$ and $$A_{cd} = \frac{v_{c1} - v_{c2}}{v_{CM}} = 0$$

The common mode rejection ratio is, by definition,

$$CMRR \equiv 20 \log \left| \frac{A_d}{A_c} \right|$$

such that, for each unique output (v_{c1} or v_{c2}), we get $CMRR \cong 20 \log \left| g_m R \right|$.

For the differential output $CMRR$ = ¥, obviously except the case where the symmetry is not perfect. Verify that, for example, if $R_{C1} = R_C$ and $R_{C2} = R_C + D\ R_C$, we get:

$$A_{cd} \cong \frac{\Delta R_C}{2R}$$

Fig. 16 illustrates a common mode input resistance definition.

Considering only half-circuit, the resistance seen by v_{CM} is 2 R_{iCM} .

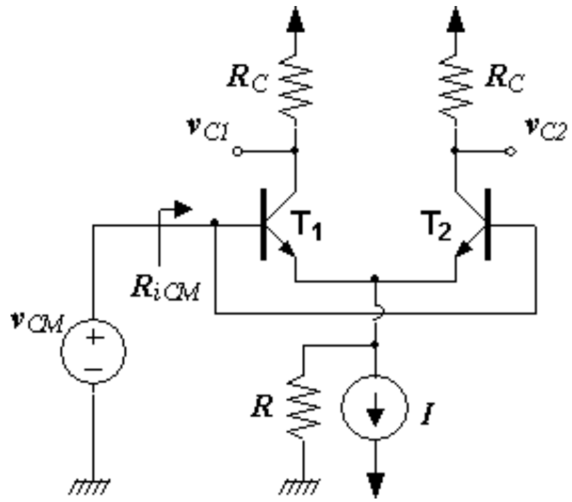


fig. 16 – Common mode input resistance

Exercise 2: *Show that*

$$R_{iCM} \cong \frac{r_\mu}{2} // \left[(\beta + 1) \left(R // \frac{r_o}{2} \right) \right]$$

and explain why in this context (where R is generally very high) it makes sense not to forget r , in general ignored for being very high.
m

Solution

2.4. Operation with arbitrary input voltages

It is convenient at this stage to (re)introduce the input signals decomposition issue, v_{B1} and v_{B2}, into two new variables: $v_D = v_{B1} - v_{B2}$ and $v_{CM} = (v_{B1} + v_{B2})/2$ (fig. 17).

Evidently, this conveys into $v_{B1} = v_{CM} + v_D/2$ and $v_{B2} = v_{CM} - v_D/2$. Let v_1 and v_2 be the signal components of v_{B1} and v_{B2}. In general, the differential pair input voltages, v_1 and v_2, corresponds neither to a differential nor to a common mode.

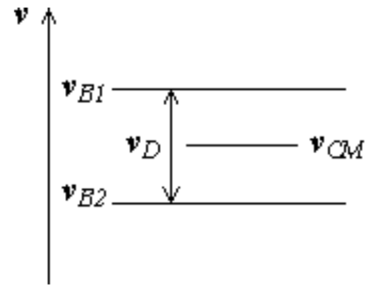


fig. 17 – Input signals

From what was said above, we have:

$$v_d = v_1 - v_2 \qquad \text{and} \qquad v_{cm} = \frac{v_1 + v_2}{2}$$

The output can be expressed as $v_o = A_1 v_1 + A_2 v_2$ as long as the signals magnitude is such that linear operation can be considered, which can further be manipulated into: $v_o = A_d v_d + A_{cm} v_{cm}$

We will have then $A_d = (A_1 - A_2)/2$ and $A_{cm} = A_1 + A_2$.

Rewriting v_o expression we get:

$$v_o = A_d v_d \left(1 + \frac{A_{cm}}{A_d} \frac{v_{cm}}{v_d}\right) = A_d v_d \left(1 + \frac{1}{CMRR} \frac{v_{cm}}{v_d}\right)$$

(where *CMRR* is expressed in non-logarithmic form) which then shows that, if the *CMRR* is sufficiently high, the output signal depends solely on the input differential component.

Because the desirable operation is precisely this, the term

$$\frac{1}{CMRR} \frac{v_{cm}}{v_d}$$

constitutes the error of the differential circuit model.

2.5. Other non-ideal characteristics

2.5.1. Input offset voltage

If the differential pair is perfectly symmetric, with the output voltage taken between the two collectors (or two drains) and connecting both inputs to the ground, then $v_O = 0$. Because perfect symmetry is impossible, in fact v_O ¹ 0 is verified.

Thus, an input offset voltage can be defined as:

$$V_{OS} \equiv \frac{v_O}{A_d}$$

The asymmetry can result from the load resistor and/or, transistor characteristics dissimilitude. If the load resistors differ by DR_C (or DR_D), that is, if

$$R_{C1,2} = R_C \pm \frac{\Delta R_C}{2} \quad \text{or} \quad R_{D1,2} = R_D \pm \frac{\Delta R_D}{2}$$

results for the BJT pair: $|V_{OS}| = V_T \frac{\Delta R_C}{R_C}$

and for a MOSFET pair: $|V_{OS}| = \frac{V_{GS} - V_t}{2} \frac{\Delta R_D}{R_D}$

The relevant transistor characteristics responsible for input offset voltage, are the reverse saturation current I_S for the BJT case, and the K factor (or I_{DSS}) and the threshold voltage V_t (or V_P) for FETs case.

Thus, for a BJT pair, the offset result is:

$$|V_{OS}| = V_T \frac{\Delta I_S}{I_S}$$

and for a MOSFET pair:

$$V_{OS} = \frac{V_{GS} - V_t}{2} \frac{\Delta K}{K} \quad \text{and} \quad V_{OS} = \Delta V_t \quad \text{respectively.}$$

2.5.2. Bias current and input offset current

Given its very small values, input currents are non-relevant for the FETs differential pairs. Consequently we will only consider the case of a BJT differential pair.

In a symmetric pair, the input currents at rest are equal to:

$$I_{B1} = I_{B2} = \frac{I/2}{\beta+1}$$

This common value is called the input bias current (I_B). Due to the inevitable input asymmetry, the bias currents are in fact different. This difference is called input offset current.

$$I_{OS} \equiv |I_{B1} - I_{B2}|$$

In particular, if transistor gains b differ by Db, the offset is:

$$|I_{OS}| = I_B \frac{\Delta\beta}{\beta}$$

Up to here we have indicated a symbolic current source to bias the differential pair. It maters now to see how can that current source be realised.

Discrete circuits are going to be distinguished from integrated current source circuits.

3. Bias circuits for differential pairs

3.1. Discrete circuits

A discrete component typical constant current source (CCS) realisation is illustrated in fig. 18 for a BJT case.

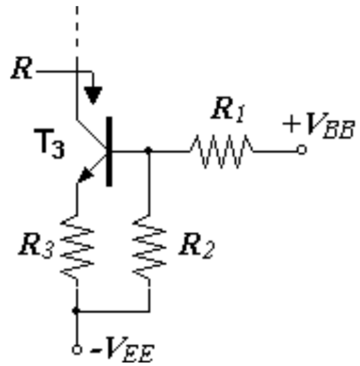


fig. 18 – Discrete differential pair bias circuit

A practical example will allow us an easier router to evaluate and project CCS circuit.

We will assume V_{BB} = 12 V and $-V_{EE}$ = -12 V, and that I_C = 1 mA is needed. Suppose that the transistor has a b = 100 and V_A = 100 V.

Taking V_B = -8 V, for I_E @ 1 mA, results R_3 = 3.3 kW.

Then, assuming I_B @ 0, we get:

$$\frac{R_2}{R_1+R_2}=\frac{4}{24} \quad \text{and} \quad R_1 = 5\,R_2$$

Choosing a current at R_1 and R_2 as being approximately 10% of I_C, (so that I_B can be neglected) we get:

$$\frac{24}{R_1+R_2}=0.1\,\text{mA} \quad \text{then} \quad R_2 = 40\text{ kW} \quad \text{and} \quad R_1 = 200\text{ kW}.$$

Exercise 3: *Find the source output resistance, R, having in mind the value of r_o and that the transistor has an emitter resistor R_3.*

Answer

Solution

3.2. Integrated circuits

The resistor values required by the previous setting are impractical for integrated circuits. On the other hand, good matching transistors are easy and economic to fabricate. Furthermore, integrated circuits using exclusively MOS technology (in particular CMOS) really excuse the use of resistors.

This way, a common technique utilised in integrated circuits to realise CCS is the current mirror. The basic current mirror with MOSFET is shown in fig. 19.

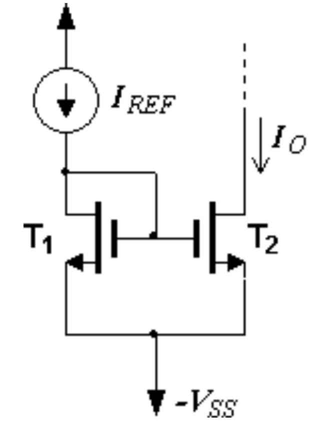


fig. 19 – MOSFET basic current mirror

If both transistors are exactly matched, and since V_{GS} is the same for both transistors, their currents will be equal. In fact, taking into account the channel length modulation, this equality is only verified if $V_{DS2} = V_{DS1} = V_{GS}$. This way, the mirror's output resistance, r_{o2}, is a quality parameter.

If both threshold voltages are the same, but different K factors are used, then

$$I_{REF} = K_1 \left(V_{GS} - V_t\right)^2 \quad \text{and} \quad I_O = K_2 \left(V_{GS} - V_t\right)^2$$

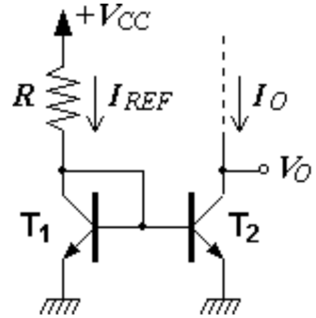
results in:

$$I_O = \frac{K_2}{K_1} I_{REF} = \frac{(W/L)_2}{(W/L)_1} I_{REF}$$

This expression shows that ratios different from the unit transfer current I_O / I_{REF} ratio are attained by a simple actuation over the transistors' geometry.

The basic BJT current mirror configuration is shown in fig. 20, where:

$$I_{REF} = \frac{V_{CC} - V_{BE}}{R}$$



Assuming T_1 º T_2, neglecting the effects of b and r_o, and since $V_{BE1} = V_{BE2}$, results $I_O = I_{REF}$.

fig. 20 – BJT basic current mirror

If the effect of b is taken into account, it is easily verified that:

$$\frac{I_O}{I_{REF}} = \frac{1}{1+2/\beta}$$

which shows that the error is made smaller with bigger b.

Simultaneously, when used as a CCS the circuit's output resistance is only r_o, a value that can be insufficiently high. Hence, the modifications usually made to the basic current mirror aim to overcome the limitations resulting from finite b and r_o.

The use of an extra transistor (T_3, in fig. 21) or the use of Wilson and Widlar configurations, shown in figs. 22 and 23 respectively, are ways to improve the referred characteristics.

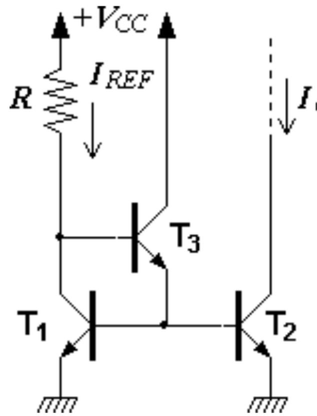


fig. 21 – Base current compensation current mirror

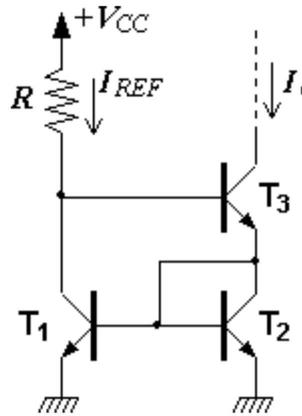


fig. 22 – Wilson's mirror

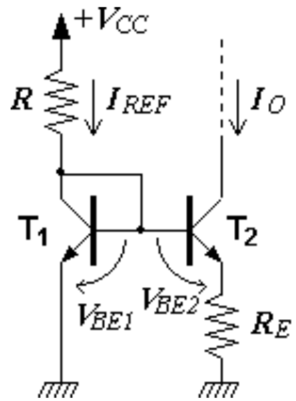


fig. 23 – Widlar's source

Exercise 4: *Find I_O and/or R_O for the following configurations:*

a) fig. 21

b) fig. 22

c) fig. 23.

Answer

Solution

The current mirrors output resistance made with MOS can also be increased using Wilson or cascode configurations.

4. Improving the bandwidth

Recall that the amplifier bandwidth refers to the frequency range within which the gain remains almost constant. We call (lower and upper) cut-off frequencies to those range limits. The criterion utilised to define these frequencies corresponds to the measure of the point where the maximum gain decreases by 3 dB, i.e., about 30% gain value decrease (3 dB means halving the electric power, which from the voltage point of view corresponds to $1 / \sqrt{2}$ @ 0.707).

At the lower limit, i.e., at low frequencies, capacitive coupling utilisation is responsible for the gain. So, when direct coupling is used, such as with integrated OpAmps, usually there is no gain decrease at low frequencies, accordingly the lower cut-off frequency is zero.

However, at high frequencies, due to transistor's intrinsic capacitive effect the gain decrease is unavoidable. Otherwise infinite frequencies would imply electrons (or other carriers, such as holes in *p* type semiconductors) infinite accelerations, and therefore infinite forces would be present, which are obviously impossible in Nature. The upper cut-off frequency depends not only on the transistors characteristics and quiescent point but as well on the chosen circuit configuration.

Then, in a direct coupling amplifier, the bandwidth coincides with the upper cut-off frequency.

4.1. CE configuration bandwidth

The CE behaviour at high frequencies is of special interest to study the differential pair, because, as we have seen before, the differential pair is somehow equivalent to a CE montage. From the three basic configurations, it is precisely the CE that has the smallest bandwidth, i.e., it has the smallest upper cut-off frequency.

The reason for this poorer behaviour at high frequencies can easily be found through a simplified analysis of the high frequency equivalent circuit of fig. 24, where r_o was ignored and, for the sake of simplicity, we have also omitted the base biasing mesh.

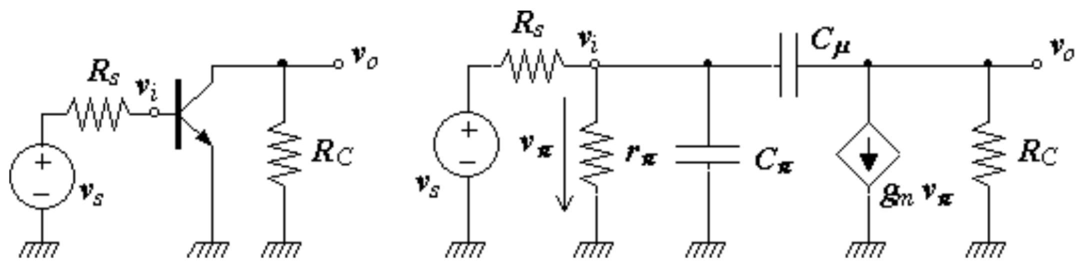


fig. 24 - CE high frequency equivalent circuit

Exercise 5: *Verify through the equivalent circuit nodal analysis that the gain expression is:*

$$\frac{v_o}{v_s} = \left(-g_m R_C \frac{r_\pi}{r_\pi + R_s}\right) \frac{1-\left(s\,C_\mu / g_m\right)}{1+s\left\{R\left[C_\pi + \left(1+g_m R_C\right)C_\mu\right] + R_C C_\mu\right\} + s^2 R\, R_C C_\pi C_\mu}$$

where $R = r_\pi \,//\, R_s$.

Notice the following points:

- *the first factor (inside parenthesis) is the MF gain, which in the model at analysis, can be obtained making* $s = 0$;
- *the expression has a zero at* $s = g_m / C_m$ *(notice that, indeed, at that frequency,* $v_o = 0$, *since the current in* C_m, *i.e.,* $s\,C_m\,v_p$, *equals* $g_m\,v_p$ *thus there is no current in* R_C *– see text);*
- *if we reckon that the denominator form is*

$$1 - s\left(\frac{1}{\omega_1} + \frac{1}{\omega_2}\right) + s^2 \frac{1}{\omega_1 \omega_2}$$

we easily conclude that the first pole is essentially equal to the inverse of the coefficient of s, once the second one is much higher.

Solution

Part of the answer, indicated in Exercise 5, can be obtained in a simplified manner with the help of Miller's theorem to the C_m capacitor, considering the midband gain value (A_{MF}).

Indeed, observing fig. 25, one can notice that the gain, in spite decreasing with frequency, little differs from the midband value in the vicinity of the first pole. Therefore, this value can be used to give an approximate value of the first pole frequency. On the other hand, it should be clear that it is an absurd to use the midband value for higher frequencies.

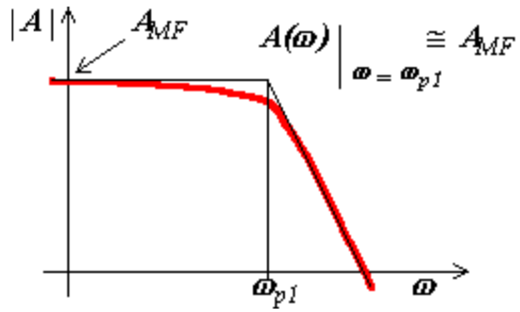


fig. 25 – Midband gain and first pole

Thus, the resulting schematic (fig. 26) is valid only to determine the bandwidth (w_H @ w_{p1}), and not the frequency response in total. Besides, it is notorious that the zero disappears in this analysis.

From fig. 26 we get

$$C_1 = C_\mu(1-K) \quad , \quad C_2 = C_\mu\left(1-\frac{1}{K}\right) \quad \text{and} \quad K = \frac{v_o}{v_i} \equiv \frac{v_o}{v_\pi}$$

The *K* value is easily obtained:

$$K = -g_m R_C$$

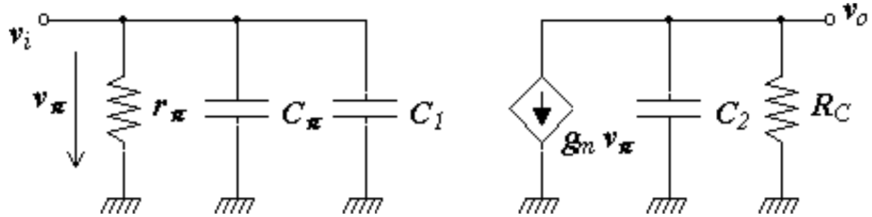


fig. 26 – HF equivalent circuit of the CE montage simplified by application of Miller's theorem

Since it is a large negative value, results:

$$C_1 \cong g_m R_C C_\mu \quad \text{and} \quad C_2 \cong C_\mu$$

Then, the time constants associated with both independent capacitors are:

$$\tau_1 = R\left(C_\pi + g_m R_C C_\mu\right) \quad \text{and} \quad \tau_2 = R_C C_\mu \quad \text{with} \quad R = r_\pi \,//\, R_s$$

and corresponding poles $\omega_1 = \frac{1}{\tau_1}$ and $\omega_2 = \frac{1}{\tau_2}$

Since in general, $w_1 << w_2$, the band limit may be considered coincident with w_1 :

$$\omega_H \cong \omega_1 = \frac{1}{R\left(C_\pi + g_m R_C C_\mu\right)}$$

On the other hand, the middle-frequency gain approximation used does not allow the identification of w_2 as the second pole of the original circuit.

A more accurate estimation for the first pole and also for the second one can be obtained, although more onerously, using the time constants method.

Note, as reference, that C_p and C_m have typical values in the order of tens and unities of pF, respectively. Besides the fact that C_m is small, its actual contribution is large because the capacitor value is multiplied by the configuration gain. This is known as the Miller multiplicative effect.

Let us make a reference to the zero. In fig. 24 schematic, the output voltage is annulled when the C_m capacitor current is equal to the current source current, i.e., when the current in R_C is zero. Then,

$$\left(v_\pi - v_o\right) s C_\mu = g_m v_\pi \quad \Rightarrow \quad s = \frac{g_m}{C_\mu}$$

This is the frequency of the zero, which coincides with the calculated value in Exercise 5. However, one should note that, given the capacitor values and assuming g_m in the order of 100 mA/V, the zero will be situated at a frequency much higher than the poles. At the present point this does not seem of great importance however, attention should be called upon the fact that the zero is located on the right hand side of the S plane (it is real and positive). Unexpectedly, this zero introduces a phase delay and not a delay advance. In this perspective behaves as a pole on the left hand side of the S plane.

In the common base and common collector configurations the Miller multiplicative effect does not exist. The last has the C_p capacitor between two nodes with slightly less than one positive gain, and the former has both capacitors to ground: the Miller effect is then out of the question. In this way, both configurations present much higher upper cut-off frequencies. It is known that in a given configuration the gain bandwidth product is approximately constant - if the gain increases the bandwidth diminishes. From all considered configurations, only the CE configuration shows both bigger than one current and voltage gains. The CC configuration has unit voltage gain and BC has a unit current gain. Thus, in a certain way, it is “natural” that the existence of two large gains make the bandwidth diminish.

From this analysis results a relatively poor high frequency behaviour for the CE configuration (thus, also for the differential pair), which needs to be improved.

One configuration with a CE equivalent voltage gain but larger bandwidth is the cascode pair.

4.2. CE-CB Cascode pair

Fig. 27 (a) represents a biasing scheme for the cascode pair and in (b) the equivalent circuit for signals, where $R_B = R_1 // R_2$.

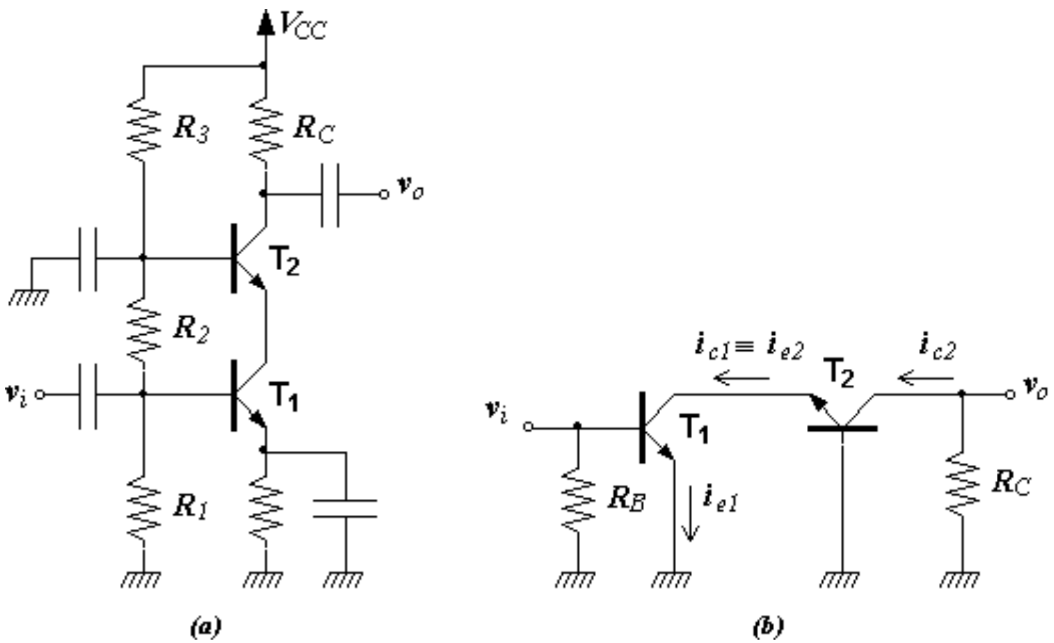


fig. 27 - CE-CB cascode pair; (a) bias circuit; (b) small signal equivalent circuit

Low frequency analysis of fig. 27 schematic gives:

$$v_o = -R_C i_{c2} = -\alpha R_C i_{c1} = -\alpha^2 R_C i_{e1} = -\alpha^2 R_C \frac{v_i}{r_e} = -\alpha g_m R_C v_i \cong -g_m R_C v_i$$

which insights that an equivalent CE v_o / v_i gain can be built with an equal transistor biased at the same DC operating point.

However a difference is in favour of the cascode configuration.

In fact, a large R_C is adopted when a large gain is needed. If R_C is sufficiently large, the $r_o >> R_C$ approximation may no longer be acceptable. Then for a CE we should consider:

$$A_v = -g_m\left(r_o \,//\, R_C\right)$$

If $R_C >> r_o$, the maximum gain is given by $-g_m r_o$.

To examine what takes place with the cascode configuration, let us determine G_m and R_o relatively to the equivalent model of fig. 27 (a) and represented in fig. 28.

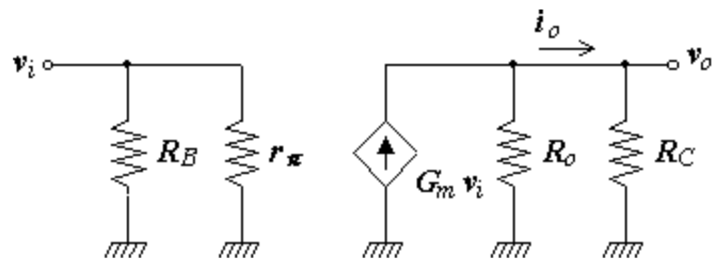


fig. 28 - Cascode pair equivalent circuit

Calculating G_m, gives:

$$G_m \equiv \left.\frac{i_o}{v_i}\right|_{v_o=0} = -\frac{i_{c2}}{v_i} = -\frac{\alpha i_{c1}}{v_i} = -\frac{\alpha^2 i_{e1}}{v_i} = -\frac{\alpha^2}{r_e} = -\alpha g_m \cong -g_m$$

To calculate R_o, fig. 29 is used.

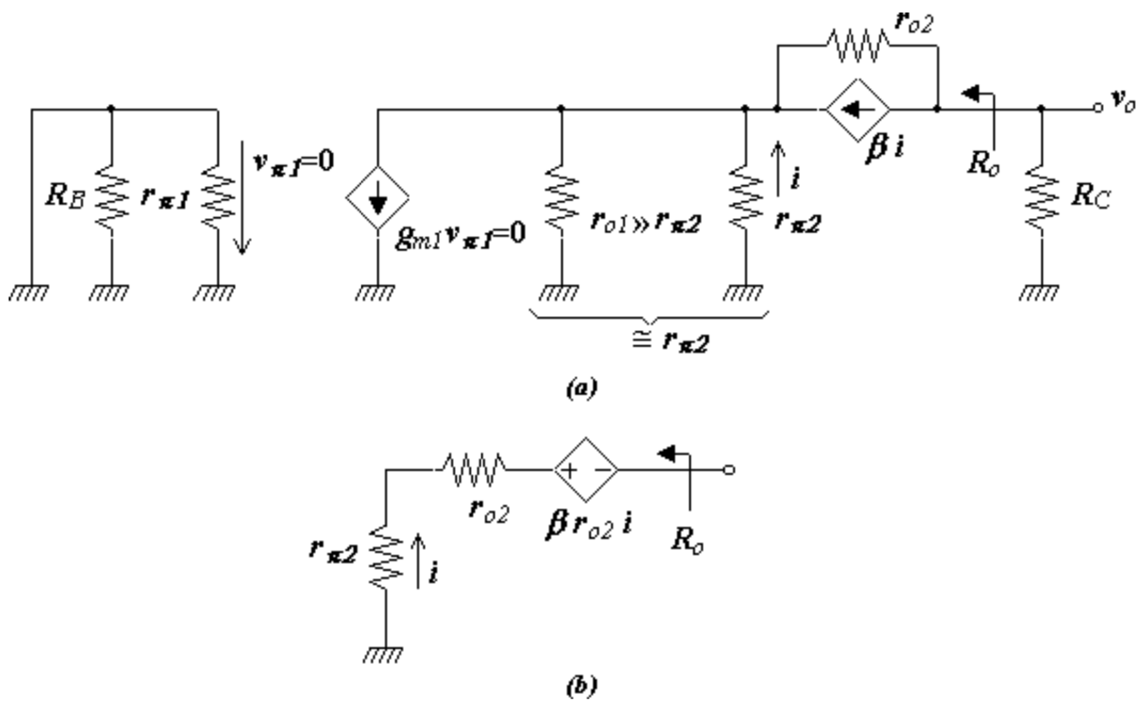


fig. 29 - Evaluation of output resistance R_o; (a) Deactivating the independent sources; (b) Circuit simplification

A deactivation condition was imposed to the independent sources in fig. 29 (a), which annuls the fonte $g_{m1} v_{p1}$ current source. Given that $r_{o1} >> r_{p2}$, then the parallel is approximately r_{p2}. Finally, applying the Thévenin's theorem results in fig. 29 (b) schematic, where the output resistance can immediately be found to be:

$$R_o = r_{\pi 2} + (\beta + 1) r_{o2} \cong \beta r_o$$

where it was considered $r_o = r_{o1} = r_{o2}$ (equal transistors with the same operating point). Then for the voltage gain we get:

$$A_v = G_m (R_o \,//\, R_C) = -g_m (\beta r_o \,//\, R_C)$$

Hence the maximum gain value will be $-g_m \beta r_o$, which is considerably larger than the common emitter gain.

As mentioned above, the cascode bandwidth is larger than the equivalent common emitter. Let us check why with a simplified qualitative analysis.

The cascode second stage is a common base amplifier, which frequency response is very good. So, it is the first stage, a common emitter, that will primarily condition the high frequency response. The CE lower cut off frequency results from the Miller multiplicative effect over the C_{m1} capacitor. However, because the first stage load is the second stage low input resistance (r_e), the Miller multiplicative factor will be solely:

$$1-K=1-(-g_m r_e)=1+1=2$$

This way, the upper cut-off frequency of the circuit will be considerably larger than the upper cut-off frequency of a CE.

4.3. CE-CB complementary cascode

Fig. 30 (a) represents the biasing scheme of a complementary cascode pair and in (b) the equivalent circuit for signal analysis.

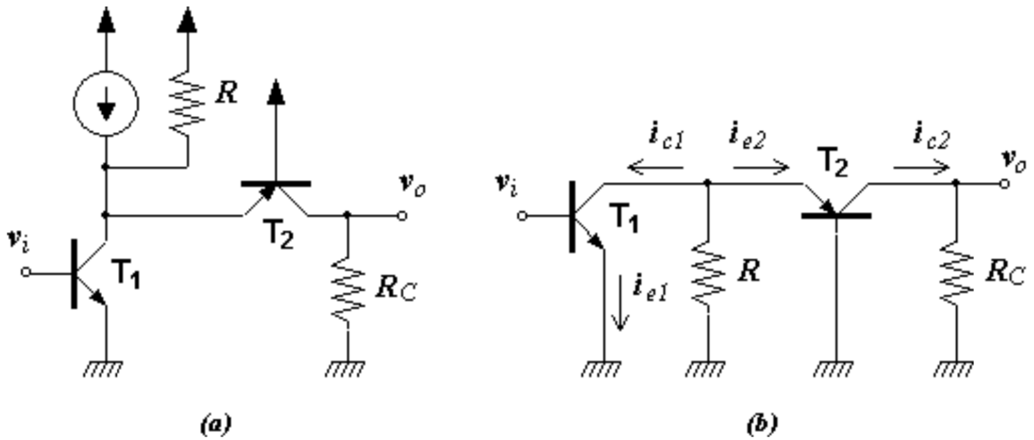


fig. 30 - CE-CB complementary cascode; (a) Bias circuit; (b) Small signal equivalent circuit

This configuration utilizes a *npn* and *pnp* transistors, which signals equivalent model is the same as last configuration (the non-complementary transistor cascode). Hence, the schematic of figs. 28 e 29 apply here.

Recall the fact that nothing changes in terms of signal functionality whichever the transistor is *pnp* or *npn*. The sole change relates with the need for a dc current to source the collector of T_1 and the emitter of T_2 simultaneously. The change to the signal circuit parameters is minimal and negligible since the resistance associated with the current source is generally much larger than r_{e2} with which will be in parallel to ground. However it may happen that I_{E1} ¹ I_{E2} which can lead to different parameters for both transistors.

Regarding everything else, all the reminding signal analysis is then still valid.

This configuration presents another advantage of great interest to the multistage amplifiers architecture, such as the case of OpAmps: the displacement level between the input and output, observed in the canonical cascode, can be annulled. In fact, this last presents a displacement level of:

$|V_{CE2}|+|V_{CB1}|$, while the complementary cascode is solely: $-|V_{CE2}|+|V_{CB1}|$

4.4. CC-CB complementary cascode

This configuration utilizes a *npn* and *pnp* transistors, which signals equivalent model is represented in fig. 31.

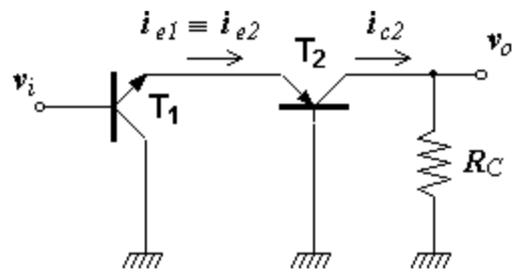


fig. 31 – CC-CB complementary cascode – small signal equivalent circuit

Assuming transistors with identical characteristics, biased at the same static operating point, the analysis leads to:

$$v_o = R_C i_{c2} = \alpha R_C i_{e1} = \alpha R_C \frac{v_i}{2r_e} = \frac{g_m}{2} R_C v_i$$

then $A_v = \frac{g_m}{2} R_C$, that is, the gain is positive (non-inverting circuit) with half a value of the CE-CB cascode gain.

However, note that in compensation the input resistance doubles the CE-CB cascode input resistance value: $R_i = 2r_\pi$.

Let us calculate now the maximum gain possible. The G_m calculation is trivial and leads to:

$$G_m = \frac{g_m}{2}.$$

Fig. 32 will be utilised for the R_o calculation. Two essential steps to find the output resistance of fig. 31 circuit, using the circuit transformations method, are represented in fig. 32. It is assumed that the source resistance, R_s, is negligible in face to r_{p1}. If this is not true, r_{p1} needs to be replaced by $R_s + r_{p1}$, which will result in a slightly larger output resistance. Thus, the value found bellow should be faced as a lower limit of a more general output resistance value.

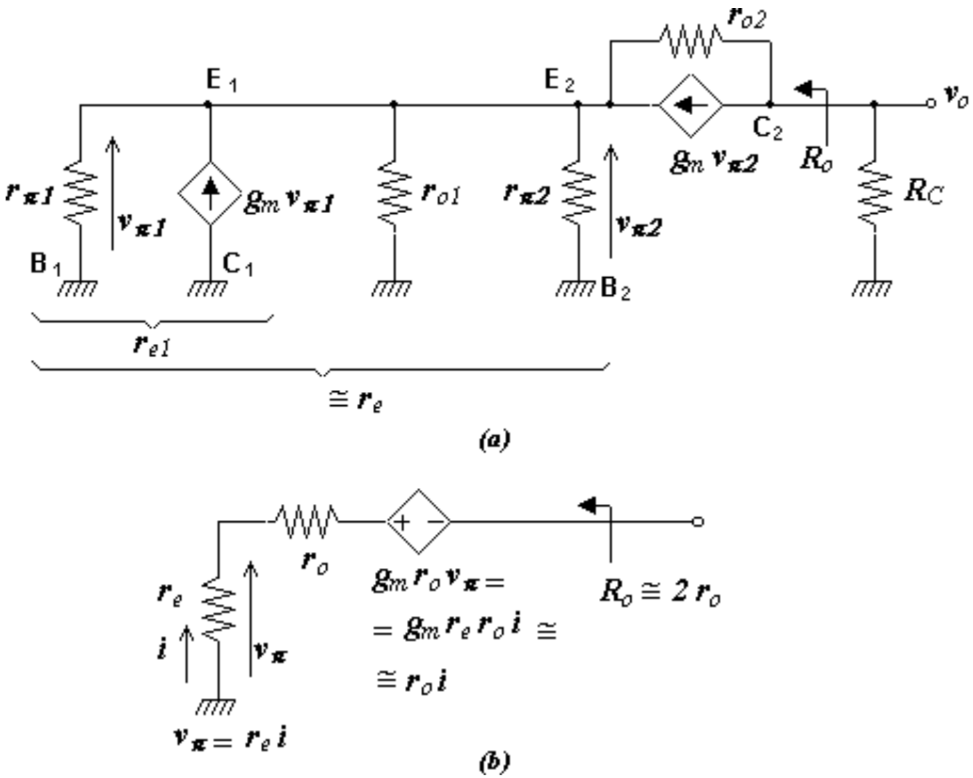


fig. 32 - Evaluation of output resistance R_o; (a) Deactivating the independent sources; (b) Circuit simplification

Exercise 6: *Find the output resistance, R_o , using the traditional method to calculate a resistance between two nodes.*

Solution

Under these conditions the maximum gain will be $A_v = g_m\, r_o$, which is equivalent to the common emitter gain.

Concerning bandwidth, one might evaluate it in a simple way. Note that capacitor C_{m1} is connected to the ground, as well as C_{p2} and C_{m2} (see fig. 33).

On the other hand, capacitor C_{p1} connects two nodes with a gain that can easily be found to be ½.

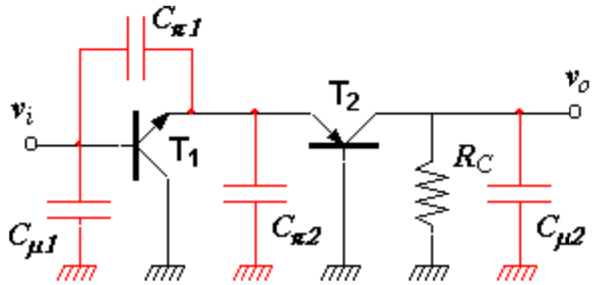


fig. 33 – Capacities in the CC-CB montage

This gain is independent of frequency and means that the Miller's theorem can be applied rigorously, i.e., without the usual restriction that results from the approximation to the midband gain. In this way, the following fig. 34 schematic results.

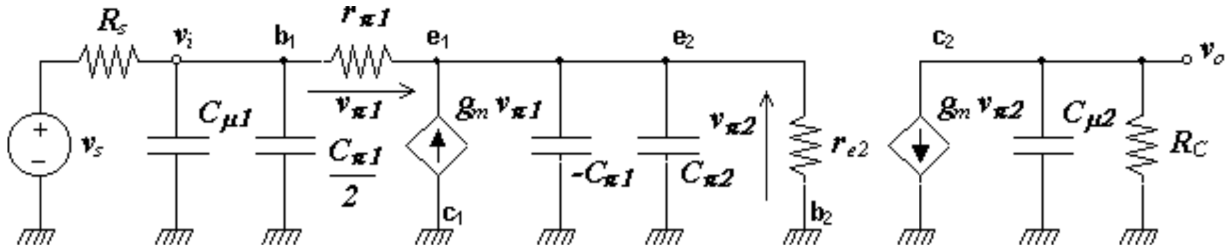


fig. 34 – CC-CB montage equivalent circuit applying Miller's theorem to C_{p1}

Since $-C_{p1}$ and C_{p2} annul each other, the circuit only presents two independent capacitances, which time constants are:

$$\tau_1 = \left(C_\mu + \frac{C_\pi}{2}\right)\left(R_s \,//\, 2r_\pi\right) \qquad \text{and} \qquad \tau_2 = C_\mu R_C$$

Which corresponding poles will be dominant or, at least, which will have the lowest frequency, is dependent on circuit parameters. However, it is notorious that any of them occur at a higher frequency than the common emitter and even higher than the CE-CB configuration.

One might reach this conclusion qualitatively. In reality, the CC-CB configuration is made of two stages, both with very good high frequency responses. In particular, the first stage, a common collector, has a upper cut-off frequency larger than the low-gain common emitter, such as the case of the CE-CB cascode. Equally the second stage is a common base with a very high cut-off frequency.

4.5. Cascode differential pair

The good frequency response properties found in a complementary cascode are utilized in the differential pair cascode, which schematic can be seen in fig. 35. This configuration is used as an input stage, e.g, in the 741 OpAmp.

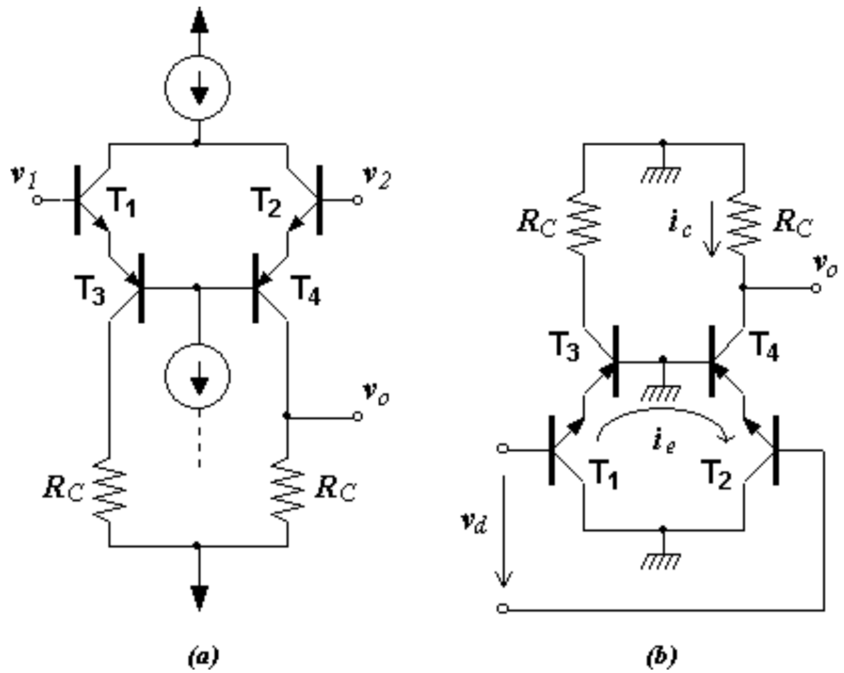


fig. 35 - Differential cascode pair; (a) Simplified bias circuit; (b) Small signal equivalent circuit

To find the voltage gain note that:

$$v_o = -R_C i_c = -\alpha R_C i_e = -\alpha R_C \frac{v_d}{4r_e} = -\frac{g_m}{4} R_C v_d \qquad \text{then} \qquad A_v = -\frac{g_m}{4} R_C$$

and from which we conclude that the gain is half of that one found in a simple differential pair. On the other hand the input resistance is double: $R_i = 4 r_\pi$.

The use of a cascode differential pair improves the general characteristics of the pair, although it seems to reduce the gain. Note, however, that the maximum gain limit is the same of a simple differential pair.

This discussion about the gain raises a question about the gain allowed by the differential pair and if it is sufficient to attain the typical values presented by a general purpose OpAmp.

5. Maximising the differential pair voltage gain

Consider the simple differential pair with single output (fig. 36) as reference.

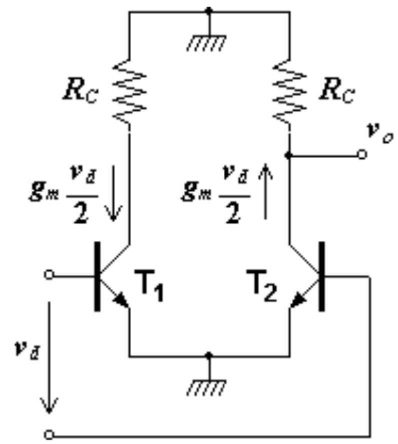


fig. 36 – Evaluation of the basic differential pair gain

The open circuit differential gain, as seen before is:

$$A_d = \frac{g_m}{2}\left(R_C // r_o\right)$$

The use of large value passive resistors are not practical so, in general, $R_C << r_o$, then:

$$A_d \cong \frac{g_m R_C}{2}$$

5.1. Differential pair with a simple active load

The gain can be considerably increased if an active load is used instead of a passive one, i.e., a current source setup with output resistance R_o , which, as seen before, can be several times larger than r_o (fig. 37).

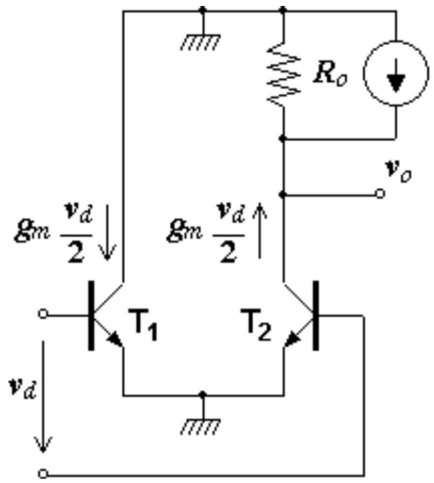


fig. 37 – Small signal equivalent circuit for the differential pair with single active load

The analysis leads to a gain value of:

$$A_d = \frac{g_m}{2}(R_o // r_o)$$

Thus, for example, if $R_o = 4\ r_o$, we get:

$$A_d = \frac{g_m}{2}(0.8 r_o)$$

5.2. Differential pair with current mirror active load

A larger value for the gain can be obtained if a current mirror is used as load, like fig. 38 shows.

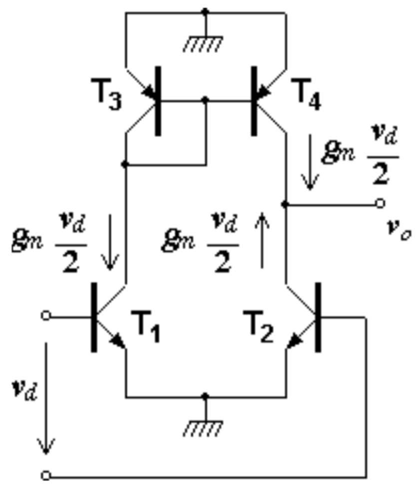


fig. 38 – Small signal equivalent circuit

The mirror effect leads to:

$$A_d = g_m(r_{o2} // r_{o4})$$

and if $r_{o2} = r_{o4} = r_o$ comes: $A_d = \frac{g_m}{2} r_o$ which is larger than what can be found with a simple active load.

This value can be further improved using a mirror with higher output resistance (fig. 39).

for the differential pair with current mirror active load

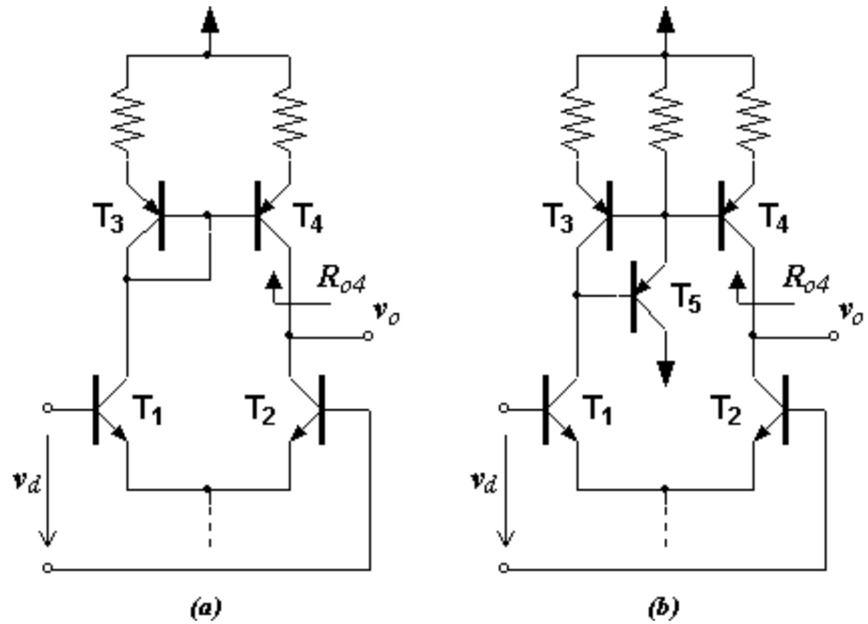


fig. 39 - Differential pair with current mirror active load; (a) symmetric Widlar's mirror; (b) base current compensation current mirror

Either using the Widlar's symmetric mirror (fig. 39 (a)), or the base current compensation mirror (fig. 39 (b)), we get:

$$A_d = g_m \left(r_{o2} \,//\, R_{o4} \right)$$

being $r_{o2} = r_{o4} = r_o$, because $R_{o4} > r_o$, then: $A_d > \frac{g_m}{2} r_o$

For example, if $R_{o4} = 4\, r_o$, then: $A_d = g_m \left(0.8 r_o \right)$

Hence, we may conclude that the open circuit maximum gain (it lowers with the load), is in the order of $g_m r_o / 2$ (it might only be slightly larger). Since

$$\frac{1}{2} g_m r_o = \frac{1}{2} \frac{I_C}{V_T} \frac{V_A}{I_C} = \frac{1}{2} \frac{V_A}{V_T}$$

then, for example, if we consider V_A = 100 V, comes: $\frac{1}{2} \frac{V_A}{V_T} = 2000$

Although it might be raised by a small amount, this value is well bellow the usual tens or hundreds of thousands gain values characteristics of OpAmps.

Even independently of other considerations, such as the ones relative to the output resistance, it is clear that a differential pair is insufficient to realize an amplifier with OpAmp like characteristics. A second stage (at least) is needed to attain the desired gain level.

The second stage needs to have a reasonable large value of gain (at least some tens) and a large input resistance to avoid gain degradation of the first stage amplifier. A low output resistance, as it is required by an OpAmp structure, is also desirable. Note however that this stage does not need to have a differential input.

5.3. One CMOS differential pair with active load

Fig. 40 shows an example of a CMOS differential pair with active load.

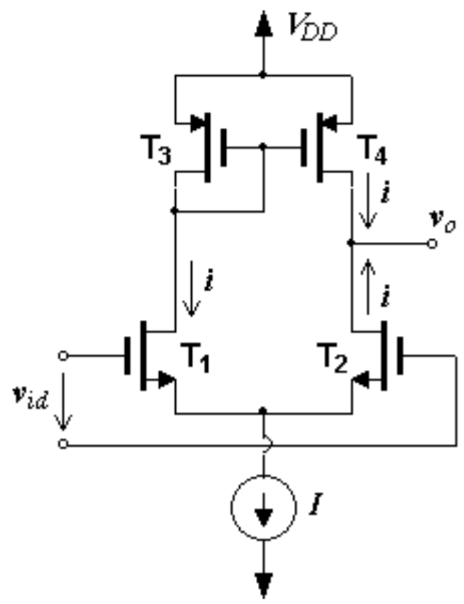


fig. 40 - CMOS differential pair with active load

The output dc voltage is, normally, established by the next stage as can be seen in the OpAmp internal circuits.

The circuit is analogous to the bipolar version. Thus, the current signal is:

$$i = \frac{g_m v_{id}}{2} \qquad \text{where} \qquad g_m = \frac{I}{V_{GS} - V_t}$$

The output voltage is: $v_o = 2i\left(r_{o2} // r_{o4}\right)$

With $r_{o2} = r_{o4} = r_o = \dfrac{V_A}{I/2}$

the voltage gain comes: $$A_v \equiv \frac{v_o}{v_{id}} = \frac{g_m r_o}{2} = \frac{V_A}{V_{GS} - V_t}$$

To get high gains, one differential cascode and one cascode current mirror can be used. However, this lowers the output signal excursion possible.

The use of FETs is specially interesting because of the very high input resistances that is allowed to get. The offset voltage is in the same order (some milivolts) of the bipolar differential pairs but, the bias currents at the input are much smaller than what is possible to make with bipolar transistors.

The major FETs inconvenience is the low transconductance and, consequently, the lower larger gain possible.

Nowadays, integrated OpAmps are fabricated using CMOS technology. The general characteristics are good and very low power voltages (1 V!) can be used with very low power consumption.

6. High voltage gain and input resistance stages

6.1. The Darlington pair – CC-CC configuration

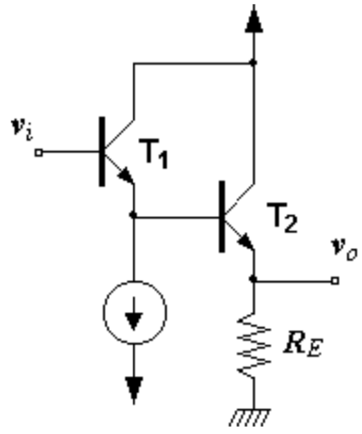


fig. 41 - Simplified schematic of the Darlington pair

Let’s consider the circuit of fig. 41, where the biasing components are omitted.

If we suppose that T_1 º T_2 and that they are equally biased, let’s compute the voltage gain and input resistance:

$$R_i = r_\pi + (\beta+1)\left[r_\pi + (\beta+1)R_E\right] = (\beta+2)r_\pi + (\beta+1)^2 R_E$$

$$v_o = R_E\, i_{e2} = R_E\,(\beta+1) i_{b2} = R_E\,(\beta+1) i_{e1} =$$

$$= R_E\,(\beta+1)^2 i_{b1} = R_E\,(\beta+1)^2 \frac{v_i}{R_i}$$

that leads to

$$A_v = \frac{v_o}{v_i} = \frac{(\beta+1)^2 R_E}{(\beta+2)r_\pi + (\beta+1)^2 R_E}$$

If b » 2, we have:

$$A_v \cong \frac{1}{1+\dfrac{r_\pi}{\beta R_E}} = \frac{1}{1+\dfrac{1}{g_m R_E}}$$

and if $g_m R_E$ >> 1, we may write the approximate value of A_v:

$$A_v \cong 1 - \frac{1}{g_m R_E}$$

which is the same expression we get for the single transistor emitter follower.

But the input resistance, if b >> 1 and R_E >> 11/g_m is: $R_i \cong \beta^2 R_E$ much larger than the value b R_E, that is the approximate value we get for a single transistor.

In the same way, the short-circuit current gain is (b +1)^2 much larger than (b +1) that the single stage has.

Finally, the output resistance is the same in both cases ($1/g_m$), if the first base is connected to ground.

Probably, the most interesting result is that the two transistor montage can be seen as one only transistor where the three terminals (B, C, E) are respectively, the first base, both collectors and the second emitter and displays a large current gain, typically b ^{2}. However, this is not completely true because in general the two transistors are very different being common that the first is a high b small signal transistor while the second is a low b power transistor.

6.2. Common Emitter Darlington configuration

In spite of what has just been said, we will admit, for the sake of simplicity, that both transistors have the same characteristics and biasing point. Then, let's consider the schematic of fig. 42.

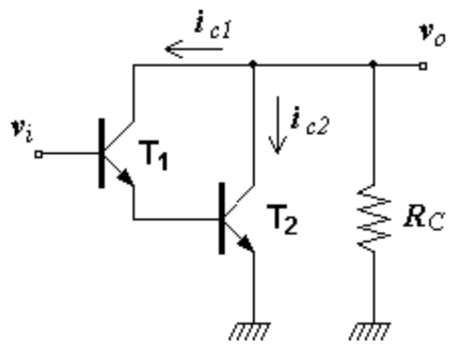


fig. 42 - Small signal equivalent circuit of CE Darlington configuration

Input resistance: $R_i = r_\pi + (\beta+1) r_\pi \cong \beta r_\pi$

Voltage gain:

$$\begin{aligned} v_o &= -R_C(i_{c1}+i_{c2}) = -R_C(\beta i_{b1} + \beta i_{b2}) = \\ &= -\beta R_C(i_{b1}+i_{e1}) = -\beta R_C(i_{b1} + (\beta+1) i_{b1}) = \\ &= -\beta(\beta+2) R_C \frac{v_i}{R_i} \end{aligned}$$

and $$A_v = \frac{v_o}{v_i} \cong -\frac{\beta^2 R_C}{\beta r_\pi} = -g_m R_C$$

We may conclude that this circuit has approximately the same voltage gain as a simple CE, but a much larger input resistance (b times larger).

However, as the internal ouput resistance is halved (r_o / 2), the maximum possible gain is smaller than what we can get with one only transistor.

Therefore, this circuit has the required characteristics for the intermediate stage of an OpAmp. However, the high frequency response is deficient. In fact, C_m of T_1 is subject to a very strong Miller effect.

6.3. CC-CE configuration

Fig. 43 represents the CC-CE circuit and its small signal equivalent. This is very similar to the circuit we just analysed (the Darlington montage) except for the fact that the two collectors are not connected.

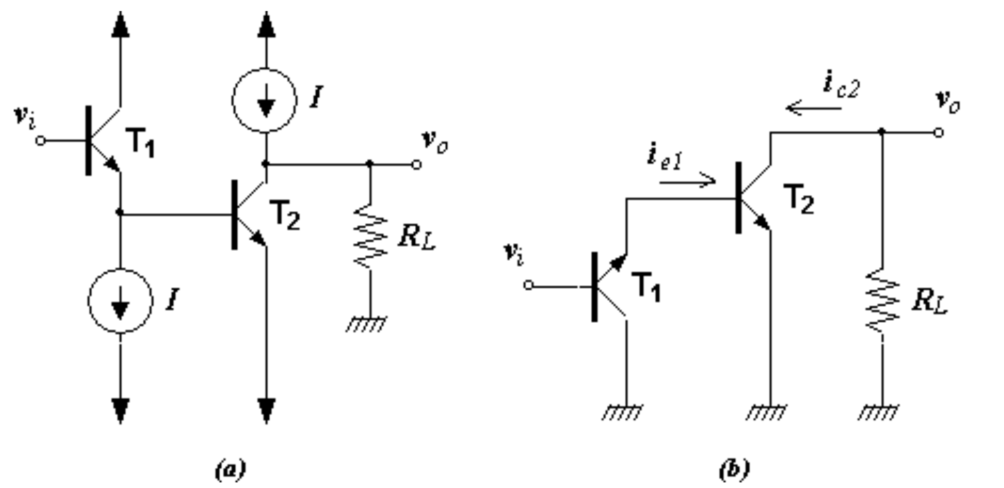


fig. 43 - CC-EC configuration; (a) simplified schematic; (b) small signal equivalent circuit

Again, for the sake of simplicity, we will admit that T_1 and T_2 are equal and equally biased.

Input resistance: $R_i = r_\pi + (\beta + 1) r_\pi \cong \beta r_\pi$

Voltage gain:

$$v_o = -R_L i_{c2} = -\beta R_L i_{b2} = -\beta R_L i_{e1} =$$
$$= \beta(\beta + 1) R_L i_{b1} \cong -\beta^2 R_L \frac{v_i}{R_i}$$

and $$A_v = \frac{v_o}{v_i} \cong -\frac{\beta^2}{\beta r_\pi} R_L = -g_m R_L$$

This circuit presents the same gain and input resistance as the CE Darlington transistor. However the maximum voltage gain is twice as large, since the output resistance (r_o) is doubled.

Though, the most significant change concerns the bandwidth. As the first stage (CE) has a good high frequency response, as we have seen before, and the Miller effect upon C_m of the second transistor does not limit much since it is charged by the low output resistance of the emitter follower the frequency behaviour of the circuit is quite good.

This is why this montage is quite common in the intermediate stage of general purpose OpAmps.

We have been referring to the common configurations of general purpose OpAmps. In general they still have a last stage that should satisfy two requirements: to have a high input resistance not to degrade the voltage gain of previous stages and have a low output resistance to be able to drive the output load. The voltage gain does not need to be high, since the two previous stages are able to provide it. Therefore, these are the characteristics we expect to find in an emitter follower circuit.

7. Output stages

The basic emitter follower presents the characteristics we have previously referred to as being desirable for an output stage but has a serious drawback: it has a very low efficiency which is important when we are dealing with power stages.

In fact, the active devices in this circuit, as in all the others that we have studied so far, are always active for the whole excursion of the input signal (the whole period, if the signal is periodic): this is what we call the Class A behaviour (as opposing other situations in which the devices can be cut-off during part of the period).

Class A has the advantage of presenting the smallest distortion but its maximum efficiency is only 25%, as we will see later on, although in certain special configurations it can be improved up to 50%.

This low efficiency is very inconvenient for the output stage in power amps once the main power dissipation is precisely in the output stage.

This is why the output stages are normally projected to work in Class B where the transistors are active, for a sinusoidal signal, during half period. This enables the efficiency to be increased to a value close to 78.5% ($\pi/4 \times 100\%$).

Naturally, a circuit with only one transistor working in class B would increase the distortion in such way that it would be more or less useless. We will see how to minimize the distortion.

The transistors can still function in other classes of which we shall now refer two:

- Class AB is characterised by keeping the devices active for more than half the period (in sinusoidal regime).

- In Class C the devices are active for less than half the period. Naturally, distortion is very high but efficiency can reach more than 90%. Therefore, this is only interesting when applied in narrow band amplifiers, that is

$$\omega_2 - \omega_1 = \text{Bandwidth} \ll \frac{(\omega_1 + \omega_2)}{2} = \text{Central Frequency}$$

Using a load impedance tuned for central frequency, it is possible to reduce distortion considerably. A typical application of this type of technique is in power radio-frequency amplifiers.

7.1. Voltage follower complementary pair

The typical configuration used in OpAmp output stages is a voltage follower pair that uses complementary transistors, symmetrically connected.

Each transistor works in class B but the way they are connected assures that there is a continuous current flow in the load.

Although this configuration may appear with slight differences, the schematic shown in fig.44 is very typical.

To understand how this circuit works, we will start with an idealized version for the components.

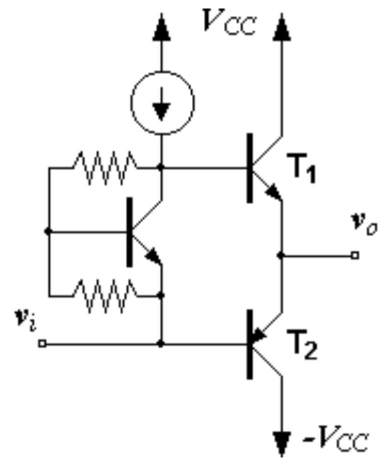


fig. 44 – Typical schematic of the voltage follower complementary pair

7.1.1. Ideal situation

Let's consider the circuit depicted in fig. 45 where T_1 and T_2 are identical, except for the fact that one is *npn* and the other *pnp*.

We shall suppose that the continuous value V_I of v_I is such that $V_O = 0$ and that the transfer characteristics of both transistors are identical (see fig.46).

When $v_i = 0$ both transistors are cut-off ($i_{c1} = i_{c2} = 0$) and therefore $i_O = i_o = 0$ and $v_O = v_o = 0$.

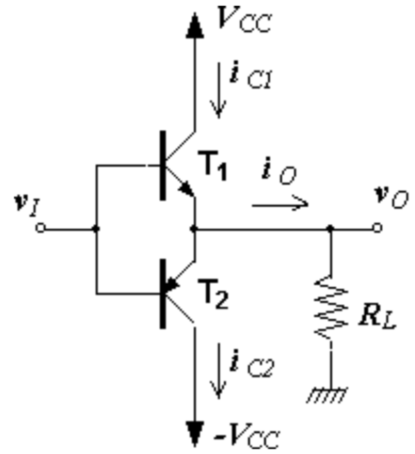


fig. 45 – Idealized schematic of the voltage follower complementary pair

Since $i_O = i_{C1} - i_{C2}$ a current will always flow in the load. Provided that none of the transistors goes to saturation, the output will be a replica of the input.

Bearing in mind that $v_{CE1} = V_{CC} - v_O$ and $-v_{CE2} = V_{CC} + v_O$, both voltages will have a sinusoidal variation identical to v_O around the mean value V_{CC}.

Fig. 47 shows the relevant voltage and current waveforms.

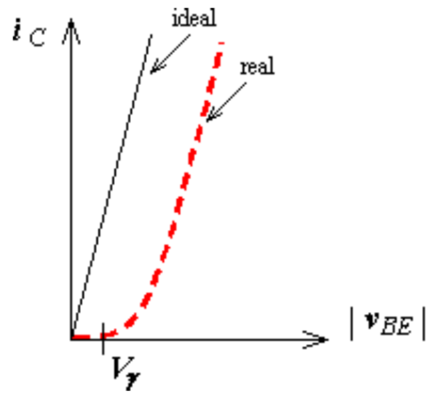


fig. 46 – Real and ideal transistor transfer characteristics

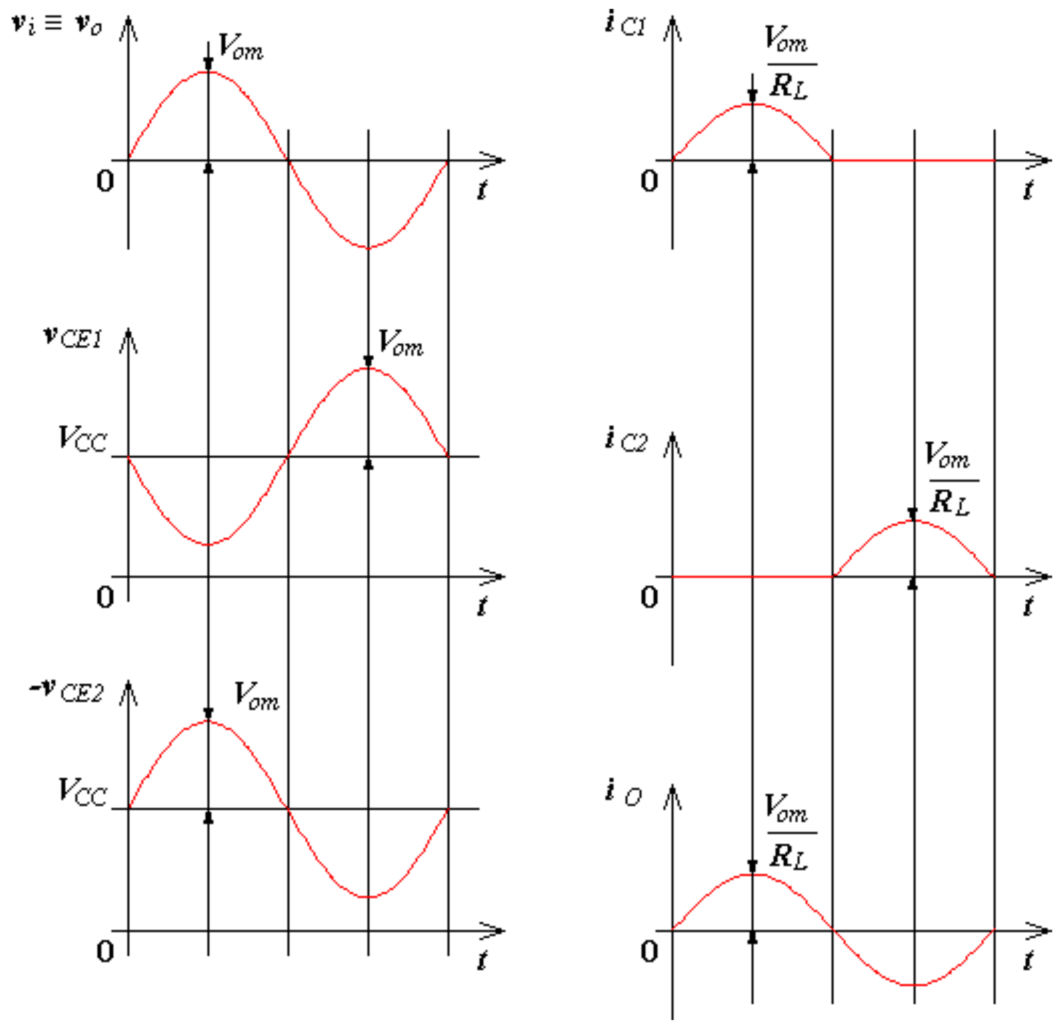


fig. 47 – Voltage and current waveforms of the voltage follower complementary pair

It is thus clear that this special configuration will allow, in the ideal case, that the circuit behaves like a voltage follower, although each transistor is in Class B, being cut-off for half of the cycle. Due to the alternate conduction of the transistors, this configuration is also known as *push-pull*.

7.1.2. Circuit behaviour with real components

For the real circuit the situation is different: it is necessary that v_{BE} gets above a certain value V_g (about 0.55 V for low power Si transistors) so that the collector current becomes significant.

We shall take, to make the analysis simpler, a piece-wise approximation to the characteristic, as shown in fig. 48.

Under these conditions, the transfer characteristic of the follower pair will have a dead zone as in fig. 49.

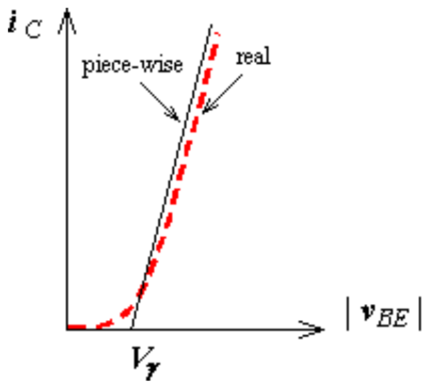


fig. 48 – Piece-wise aproximation to the transfer characteristic of a transistor

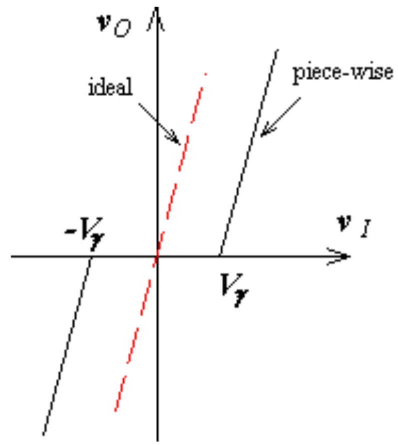


fig. 49 – Transfer characteristic of the voltage follower complementary pair

As a consequence, under a sinusoidal regime, the output will not be a sine wave, having a strong distortion around zero, known as the crossover distortion (fig. 50).

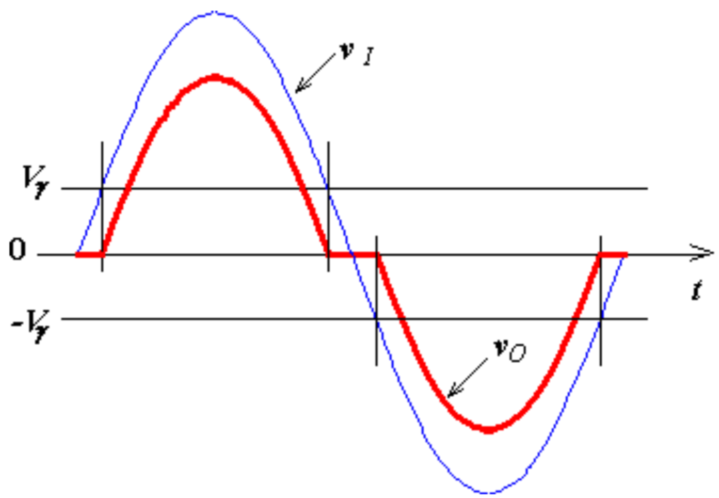


fig. 50 - Crossover distortion in the voltage follower complementary pair

In order to reduce it, both transistors should be at cut-in for a zero voltage input. To be precise, in this situation the transistors are in Class AB but so close to class B that the efficiency is only slightly smaller than in class B.

7.1.3. Compensating the crossover distortion

There is a number of possible solutions to bias the follower pair at cut-in. One of the more popular and versatile ones is the so called V_{BE} multiplier (fig. 51).

If the base current of T_3 is much smaller than the current in R_1 and R_2,

$$V = \frac{R_1 + R_2}{R_2} V_{BE} = \left(1 + \frac{R_1}{R_2}\right) V_{BE}$$

Through the choice of R_1 and R_2 we can obtain the desired value for V.

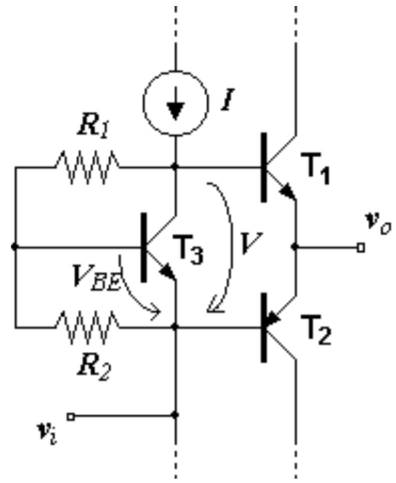


fig. 51 - V_{BE} multiplier

Exercise 7: *Evaluate the values of V_{BE} and I_C for transistors T_1 and T_2 in the circuit of fig. 51, if you have $I = 200$ mA, b $= 200$, $I_{s3} = 10^{-14}$ A, $I_{s1} = I_{s2} = 3$ ´ 10^{-14} A, and $R_1 = R_2 = 7.5$ kW.*

Answer

Solution

A different version of the V_{BE} multiplier, frequent in IC OpAmp circuits (namely in the very common 741) is depicted in fig. 52.

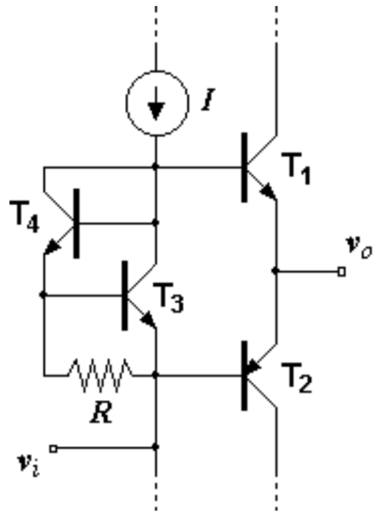


fig. 52 - Another V_{BE} multiplier

7.1.4. Understanding the V_{BE} multiplier

We have seen that the role of the V_{BE} amplifier is to suply the biaising voltage to the output transistor pair, i.e. the role of a constant voltage source. This role is better played if the resistance seen between the multiplier terminals is very small. This means that, from a signal point of view, the two bases are short-circuited.

Let's now compute its value for the circuit of fig. 51. The equivalent circuit to compute the resistance value is given in fig. 53.

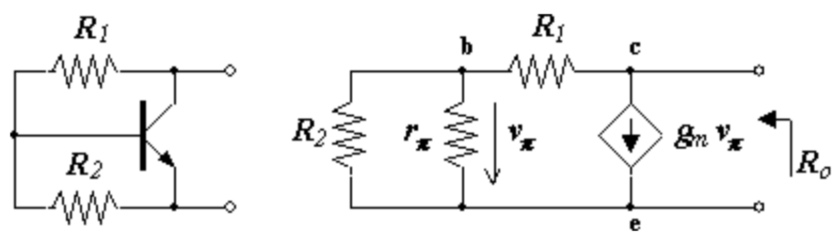


fig. 53 - Evaluation of the V_{BE} multiplier output resistance

The value of the resistance is

$$R_o = \frac{R_1 + R_2 // r_\pi}{1 + g_m (R_2 // r_\pi)}$$

and its evaluation is left as an exercise. With the values given for Exercise 7 the result is $R_o \approx 432\ \Omega$. This is a small value when compared with r_π for transistors T_1 and T_2.

Exercise 8: *Compute the value of the resistance seen between the terminals of the* V_{BE} *multiplier from fig. 52, if* $\beta = 200$, $I_{C4} = 16\ \mu A$, $I_{C3} = 160\ \mu A$ *and* $R = 40\ k\Omega$, *using the simplified* π *model for the transistors.*

Answer

Solution

So, it is an acceptable approximation to consider the V_{BE} multiplier as an ideal constant voltage source and the voltage follower pair behaves like a simple emitter follower and so its voltage gain $A_v \approx 1$ and $R_i = r_\pi + (\beta + 1) R_L$.

In fact, the situation departs from this ideal result mainly because the output stage has frequently to handle large signals which means that both the voltage gain and the input resistance vary significantly along the signal swing, because both r_π and β are a function of the collector current.

However, as the input resistance variation affects the voltage gain of the preceding stage in the inverse sense, the change of r_p is fairly compensated; there remains the variation of b but this is normally much less significant.

Cascading the three stages that we have analysed (the differential pair, the high voltage gain stage – e.g. CC-CE – and the voltage complementary pair, we obtain a complete amplifier that has the necessary characteristics to build an OpAmp (fig. 54).

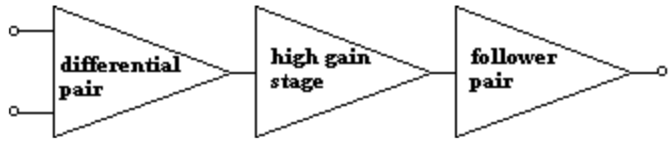


fig. 54 - Block diagram of an amplifier of the OpAmp type

However, one of the characteristics that we have only scratched is the input resistance that should be high for each stage that we analysed. In the following chapter we will go further in this respect.

8. Getting a high input impedance

Let us start by reviewing some basic transistor configurations that can lead to high input impedance.

The BJT CE as well as the FET CG configurations are to be excluded, due to the fact that R_i is inevitably low (@ $1/g_m$).

In the remaining configurations, when there is the gate of an FET as input terminal, R_i is very high but, due to a smaller g_m, the FETs, in general, display a smaller gain.

The CC configuration presents a high input resistance but a unit voltage gain. Therefore, whenever we need a higher voltage gain it is frequently associated to a CE.

The CE configuration with an emitter resistor has also a higher R_i and a moderate voltage gain and it is sometimes a useful montage when the circuit requirements are not very demanding. Among the configurations we have been seeing to behave as input stages with moderate gain, in the CE configuration, R_i equals r_p. Having a differential pair increases it to 2 r_p and even with a differential cascode it is at most 4 r_p. Is this enough?

8.1. The CE input resistance

The value of r_p is

$$r_\pi = \frac{\beta V_T}{I_C}$$

which means that its value depends upon the collector current. If we keep I_C low enough, r_p can be fairly high.

Let's take as an example b = 200 and I_C = 10 mA, and we will have:

$$r_\pi = \frac{200 \times 25 \times 10^{-3}}{10 \times 10^{-6}} = 500\,\mathrm{k}\Omega$$

If we have a differential pair in which both transistors have the above static values, R_{id} = 1 MW.

We should bear in mind that we have always ignored r_m. That can be done if R_L is not very large. However, if we want to have very high voltage gain, R_L may be very large and r_m may have to be considered. Take the example of fig. 55 to evaluate R_i.

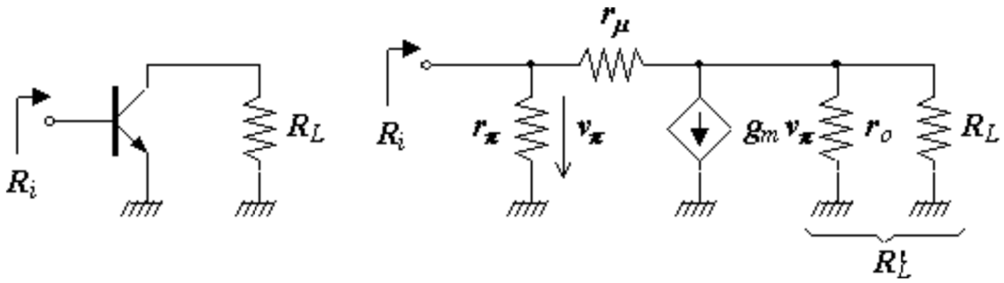


fig. 55 - Evaluation of the common emitter input resistance

The value we get is $$R_i = r_\pi // \left(r_\mu + R'_L\right) // \frac{r_\mu + R'_L}{g_m R'_L}$$

which is left to be obtained as an exercise. In any case $$r_\mu + R'_L » \frac{r_\mu + R'_L}{g_m R'_L}$$

because $g_m R'_L$ is high. Indeed, if for instance I_C = 10 mA, V_A = 100 V, b = 200 and R_L is high, close to r_o, $g_m R'_L$ = 2000.

Then $$R_i \cong r_\pi // \frac{r_\mu + R'_L}{g_m R'_L}$$

It can be shown that r m ³ b r_o and for modern IC BJTs, r m @ 10 b r$_o$.

Taking again, for simplicity, $R_L = r_o$, we get:

$$\frac{r_\mu + R'_L}{g_m R'_L} = \frac{10\beta r_o + \frac{r_o}{2}}{g_m \frac{r_o}{2}} \cong 20 r_\pi$$ and so, $$R_i = r_\pi // 20 r_\pi \cong r_\pi$$

However, for the minimum value of r_{m}, i.e., r_{m} = b r_o, we get:

$$\frac{r_\mu + R'_L}{g_m R'_L} \cong 2 r_\pi \qquad \text{and} \qquad R_i = r_\pi \,//\, 2 r_\pi \cong 0.67\, r_\pi$$

We may conclude that when we have a very high gain, the Miller effect over r_{m} may reduce the input resistance by an appreciable amount.

It should be stressed, however, that this effect is not present in other configurations, namely in the cascode.

8.2. Decreasing the input resistance of the emitter follower due to the base biasing resistors

The topic that we will now discuss is not much relevant in integrated OpAmps, where the biasing scheme is normally obtained with current sources and current mirrors. In discrete circuits, however, circuits are commonly biased through voltage dividers.

Let's consider the circuit in fig. 56, where T is a simple transistor but which, in other circuits, might be a Darlington configuration.

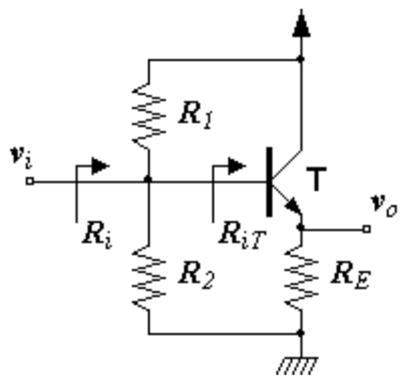


fig. 56 - Follower emitter input resistance

The transistor input resistance, R_{iT}, is $\quad R_{iT} = r_\pi + (\beta + 1) R_E$

and may be very high. For instance, if b = 100, I_C = 1 mA and R_E = 10 kW, we will have:

$R_{iT} \cong 1\text{M}\Omega$

However, the “real” input resistance for the circuit is: $R_i = R_1 // R_2 // R_{iT} = R_B // R_{iT}$

which means that to have R_i @ R_{iT} , we have to choose $R_B >> R_{iT}$. If, for instance, R_B = 10 MW, R_1 and R_2 had to be extremely large and the Thévenin voltage

$$V_{BB} = \left(\frac{R_B}{\beta + 1}\right) I_E + V_{BE} \cong 110\,\text{V}$$

would have quite an unusual value!

Let’s now consider the circuit of fig. 57(a) as well as, in fig. 57(b), its small signal equivalent, where $R_B = R_1 // R_2$.

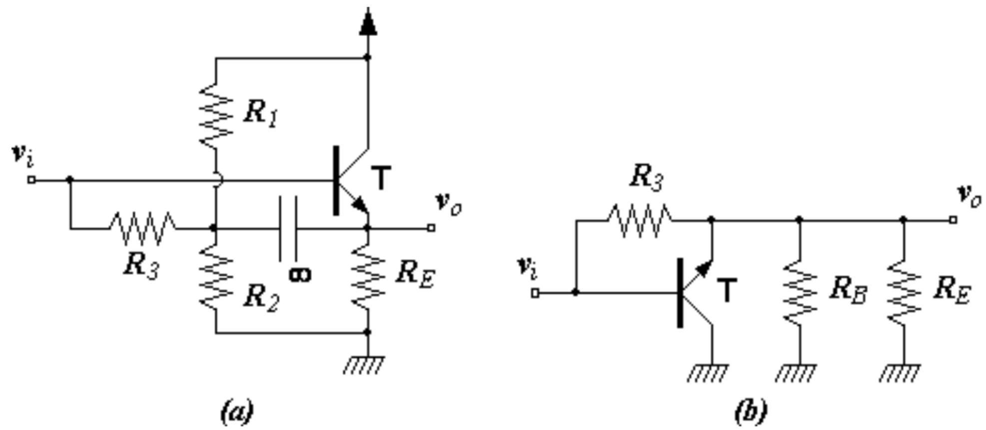


fig. 57 - Follower emitter with bootstrap efect; (a) simplified schematic; (b) small signal equivalent

Applying the Miller's theorem to R_3 we get the result depicted in fig. 58, where A_v is the voltage gain, slightly smaller than one, i.e., $A_v \cong 1 - \delta$.

Therefore $R_3/(1-A_v) \cong R_3/\delta$ will be very high and R_i @ R_{iT}.

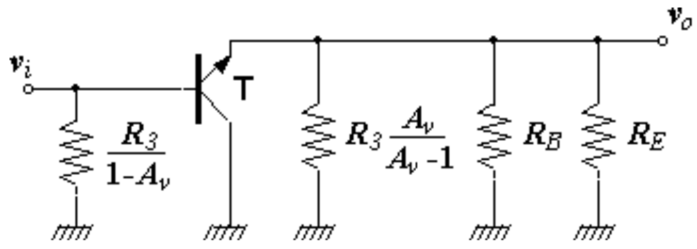


fig. 58 - Applying the Miller's theorem to the fig. 57 (b) schematic

This effect, when A_v ® +1, is known as *bootstrap*.

It should also be noted that the value of the gain and the input resistor should take into account that the effective emitter load is not only R_E, but also R_B and $R_3 A_v/(A_v - 1) \cong -R_3/\delta$. This last value is also very high and ... negative!

Let's now recall that when we have the parallel of R, a finite and positive resistance, with R', which may vary from -¥ to +¥, its value varies according to fig. 59.

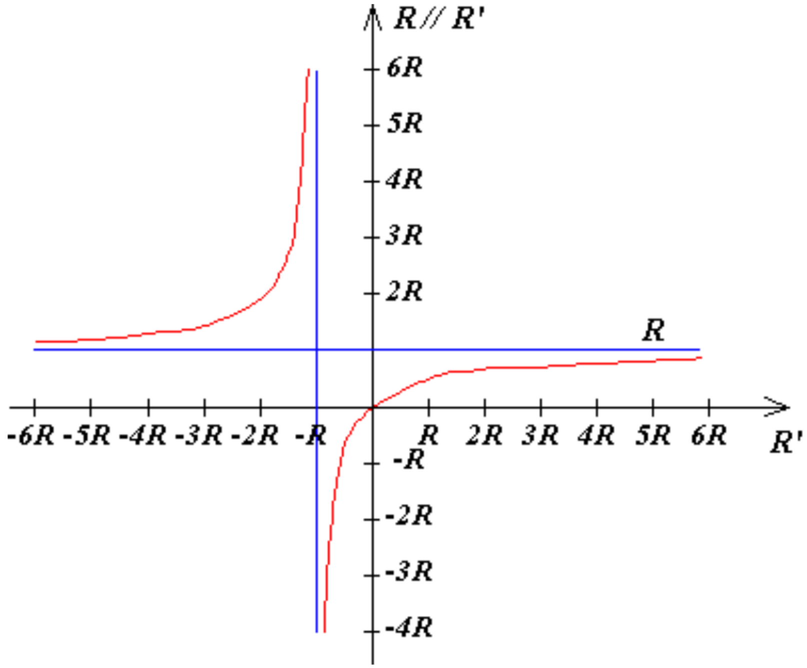


fig. 59 - Variation of the parallel of a positive and finite resistance with an arbitrary one

So, as R_E // R_B has normally a moderate value, its parallel with a very high negative resistance is only slightly larger than R_E // R_B .

We should also note that positive and negative resistance is quite normal if we are talking of dynamic values or impedance instead of resistance. An infinite impedance is obtained, for instance, with a parallel resonant L / C circuit, which is an illustration of this if we take Z instead of R.

By *bootstrapping* the biasing resistors we achieve a very high input resistance, similar to the one we see at te base of the emitter follower.

It is interesting to see how far can we go in increasing the input resistance. If R_E is the emitter resistor, we have the circuit of fig. 60.

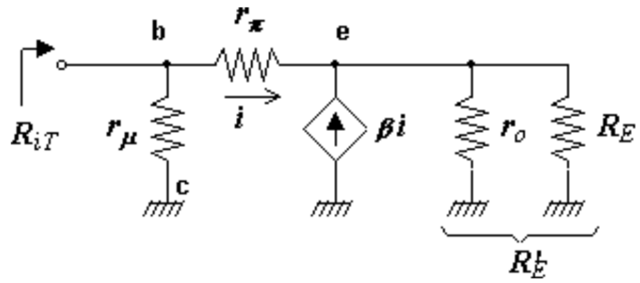


fig. 60 – Input resistance of a common collector with bootstrap effect

We can then write

$$R_{iT} = r_\mu // \left[r_\pi + (\beta+1)R'_E\right]$$

where it can be seen that r m puts a limit to the maximum value of the input resistance.

From the preceding analysis we can draw a number of conclusions concerning the procedure to adopt to achieve a high resistance at the differential input of an amplifier with a typical OpAmp structure:

- Using BJTs at the input stage, to achieve a high input resistance we should use very low biasing currents. In the 741 OpAmp, this value is approximately 10 mA.

- The use of small emitter resistors also increases the input resistance, but it reduces the voltage gain. However in precision OpAmps, which normally have a second differential amplifier, the use of emitter resistors is quite common. Another alternative is to use Darlington configurations at the input but it harms the bandwidth.

- A similar solution is used in the second differential stage of precision OpAmps, and it consists of attacking it with emitter followers with active loads (fig. 61).
  This way we get a high input resistance as well as a broad bandwidth.

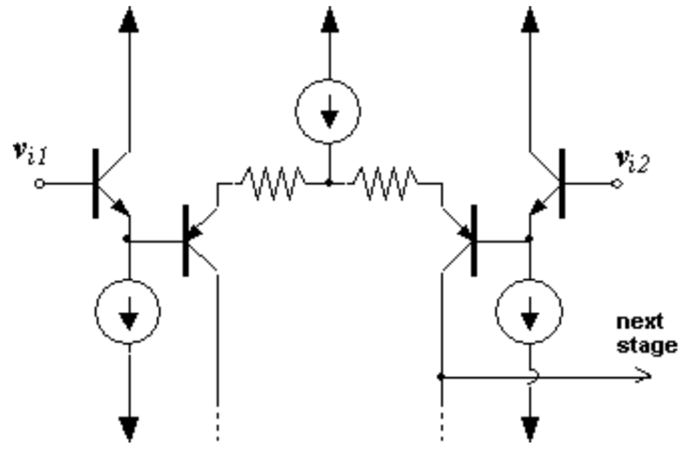


fig. 61 - Example of a second differential stage used in precision OpAmps

- Finally, using FETs instead of BJTs provides a much higher input resistance and it is common that even in bipolar technology, to have JFETs at the input of the OpAmp.

9. Analysis of a typical three stage OpAmp (mA741)

One of the most typical three stage bipolar OpAmps is certainly the mA741 developed by Fairchild but produced, today, by a large number of different brands. It is a general-purpose high gain OpAmp, useful for low frequency applications.

Its internal architecture displays most of the conventional IC stages that we have been studying.

The first stage is a differential pair using complementary cascode montages (T_1 to T_4) having as an active load a *npn* current mirror with base current compensation (T_5 to T_7).

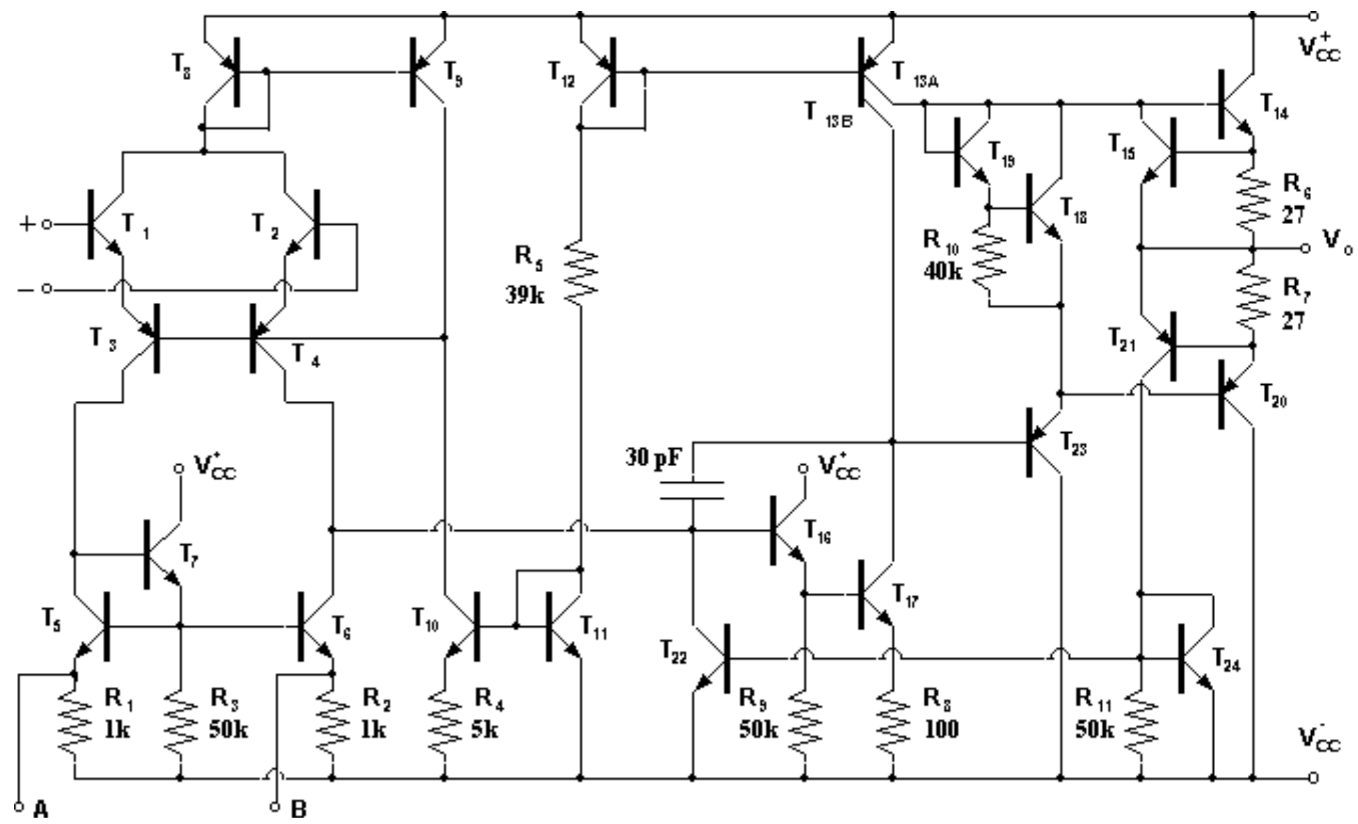


fig. 62 – Internal schematic of the mA741 OpAmp

The CC-CB cascode configuration provides a large bandwidth with small input capacitance.

The input resistance is also higher (approximately the double) than what would result from a simple differential pair with identical bias currents.The intermediate stage uses a CC-CE montage (T_{16} to T_{17}) having high input resistance, high gain and a good frequency response. The 30 pF capacitor connected between input and output of this stage provides, as will be seen later on, a Miller (pole splitting) compensation, guarantying an unconditional stability.

The output stage has the adequate high input resistance and low output one as well as good current source and sink capacity.

In this way, the fundamental cell of this stage is the emitter follower complementary pair (T_{14} to T_{20}) with crossover distortion compensation (T_{18}, T_{19} and R_{10}). This stage is preceded by another single transistor CE (T_{23}) that is used as a buffer between the second and the output stages.

Circuit bias currents are, as usual, provided by a set of current mirror configurations. T_{11}, T_{12} and R_5 establish the value of the current that is mirrored by T_{10}. The connection to the base of T_3 and T_4 and the T_8-T_9 mirror, establish the currents in the differential pair through a feedback loop.

The reference current is also mirrored from T_{12} to the double collector transistor T_{13} which can be seen as two independent transistors T_{13A} and T_{13B}.

The 741 OpAmp has still a set of extra transistors (T_{15}, T_{21}, T_{22} and T_{24}) the role of which is to protect the device from damaging output short circuits.

Terminal A and B are used for offset compensation, by means of a 10 kW potentiometer connected between A and B and the middle point connected to V_{CC}^-.

In the remaining analysis, we will take, for all the transistors (except T_{21}, T_{22} and T_{24} that have a three times larger area), $I_S = 10^{-14}$A.

The total area of T_3 is still the same but split unevenly between the two components: three fourths to T_{13B} and the remaining fourth to T_{13A}. Therefore

$$I_{S13A} = 0.25 \times 10^{-14}\ \text{A} \quad \text{and} \quad I_{S13B} = 0.75 \times 10^{-14}\ \text{A}.$$

Furthermore, we will take, for *npn* transistors,

$$b = 200 \quad \text{and} \quad V_A = 125\text{ V}$$

and for *pnp*

$$b = 50 \quad \text{and} \quad V_A = 50\text{ V}$$

Finally both for DC and AC analysis, although we only look at the internal circuit, we will always admit that a negative feedback loop is closed so that the DC output voltage is essentially zero and all the transistors are in the active region.

9.1. DC analysis

Let the supply voltages be ± 15 V and both inputs connected to ground.

From fig. 63

$$I_{REF} = \frac{30 - 0.7 - 0.7}{39\text{k}} = 0.73\text{ mA} \quad \text{and} \quad I_{11} = I_{REF}\,.$$

which results in

$$V_{BE11} - V_{BE10} = R_4 I_{10} = V_T \ln\frac{I_{REF}}{I_{10}} \quad \Rightarrow \quad I_{10} = 19\mu\text{A}$$

Symmetrically $I_{C1} = I_{C2} = I$ and as $b_N >> 1$ we have:

$$I_{E1} = I_{E2} = I_{E3} = I_{E4} \cong I \quad \text{and} \quad I_{B3} = I_{B4} \cong \frac{I}{\beta_P}$$

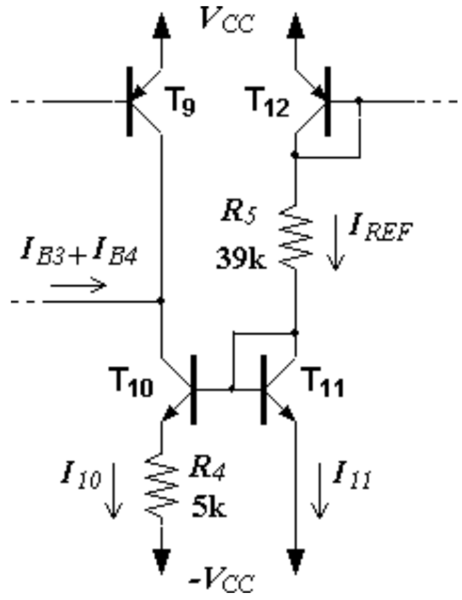


fig. 63 - Reference current

From fig. 64 we may conclude I_9 @ I_8 @ $2I$

and $$I_{10} = I_9 + \frac{2I}{\beta_P} \cong 2I + \frac{2I}{\beta_P} \cong 2I$$

and finally $I_1 = I_2$ @ $I_3 = I_4 = 9.5$ mA.

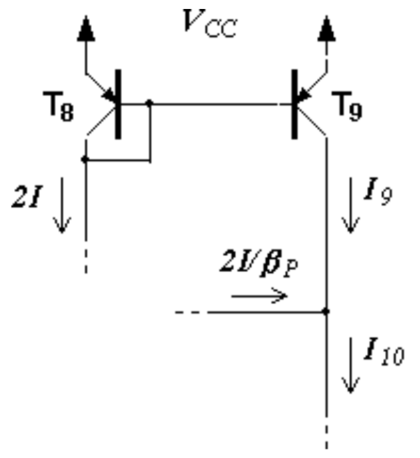


fig. 64 - Bias current of the differential pair

Transistors T_1 to T_4, T_8 and T_9 establish a negative feedback loop that stabilises I to a value approximately equal to $I_{10} / 2$. In fact, if for some reason I increases, we'll successively have

$I_8 \uparrow$ Þ $I_9 \uparrow$ and as I_{10} has a constant value

$I_{B3} = I_{B4} \downarrow$ Þ $I_3 = I_4 = I_1 = I_2 = \mathrm{I} \downarrow$

The currents in the mirror that loads the differential pair are I_5 @ I_6 @ I, as can be seen in fig. 65 and disregarding both I_{B16} and I_{B7}.

On the other hand:

$$I_7 = \frac{2I}{\beta_N} + \frac{V_{BE6} + R_2 I}{R_3}$$

where

$$V_{BE6} = V_T \ln \frac{I}{I_S} = 517 \text{ mV} \quad \text{resulting} \quad I_7 = 10.5\,\mu\text{A}$$

This shows that I_{B7} is indeed very small.

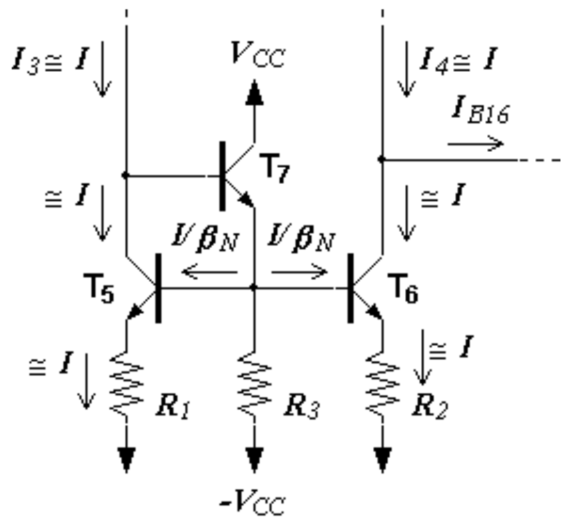


fig. 65 - Currents in the mirror

Let's now analyse the second stage (fig. 66).

Ignoring I_{B23},

we have I_{17} @ I_{13B}

and as $I_{13A} + I_{13B} = I_{REF}$ and $I_{SB} = 3$ ´ I_{SA},

I_{13B} @ $0.75\, I_{REF} = 550$ mA $= I_{17}$ the result of which is

$$V_{BE17} = V_T \ln \frac{I_{17}}{I_S} = 618\ \text{mV}$$

and

$$I_{16} \cong I_{B17} + \frac{V_{BE17} + R_8 I_{17}}{50\text{k}} = 16.2\ \mu\text{A}$$

Again, according to our approximations, we have $I_{B16} << I$.

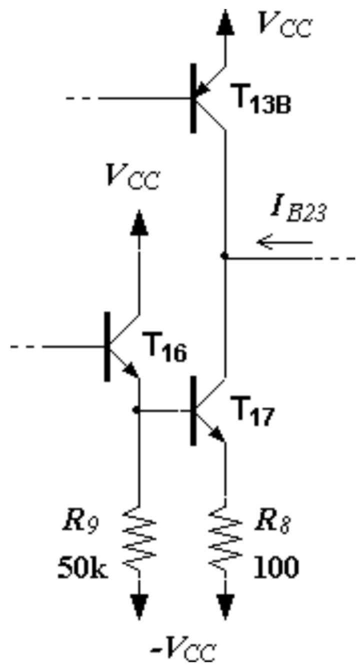


fig. 66 - Currents in the second stage

Finally, let's see the currents in the output stage (fig. 67 where, because of their very small value, we ignored the resistors R_6 e R_7).

If I_{B14} and I_{B20} are approximately zero we will have I_{23} @ 0.25 I_{REF} = 180 mA, and therefore I_{B23} = 3.6 mA, which is really much smaller than I_{17} = 550 mA.

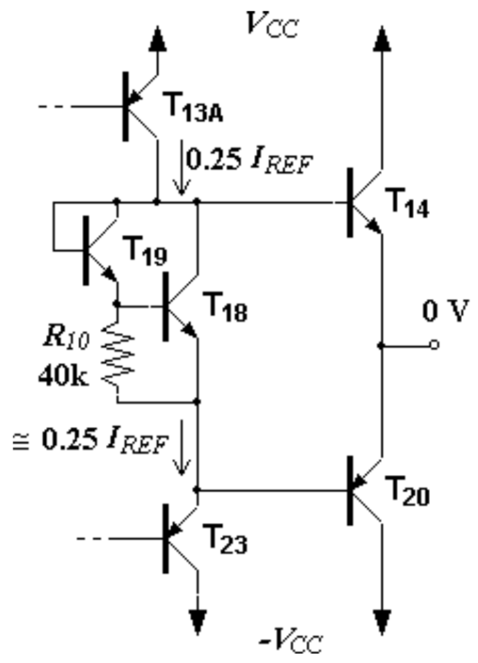


fig. 67 - Currents in the output stage

From
$$I_{19} + I_{18} \cong 180\,\mu\text{A}, \quad I_{19} = \frac{I_{18}}{\beta_N} + \frac{V_{BE18}}{40\text{k}}$$
and $$I_{18} = 10^{-14} e^{V_{BE18}/V_T}$$

we get $$V_{BE18} = V_T \ln\left[10^9 \left(18 - 2.5 V_{BE18}\right)\right]$$ and

V_{BE18} = 588 mV, I_{18} = 165 mA, I_{R10} = 14.7 mA and

I_{19} = 15.5 mA.

Then $$V_{BE19} = V_T \ln \frac{I_{19}}{I_S} = 529\text{ mV}$$

and the potential between the base T_{14} and of T_{20} is V_{BB} = 0.588 + 0.529 = 1.117 V

As $$V_{BB} = V_T \ln \frac{I_{14}}{I_{S14}} + V_T \ln \frac{I_{20}}{I_{S20}}$$ and $$I_{S14} = I_{S20} = 3\times10^{-14}\text{ A}$$

we can see that $I_{14} = I_{20}$ = 152 mA.

9.2. Small signal analysis

In the small signal analysis we will evaluate the differential voltage gain, the input differential resistance as well as the output resistance. To compute the gain we suppose that the OpAmp is loaded with R_L = 2 kW, since this is the usual situation for the gain specification in the data sheets.

Fig. 68 shows the equivalent circuit for low frequency small signals where the active load effect of the current mirror, on the differential pair, is represented by a controlled source $v_d / 4\, r_e$.

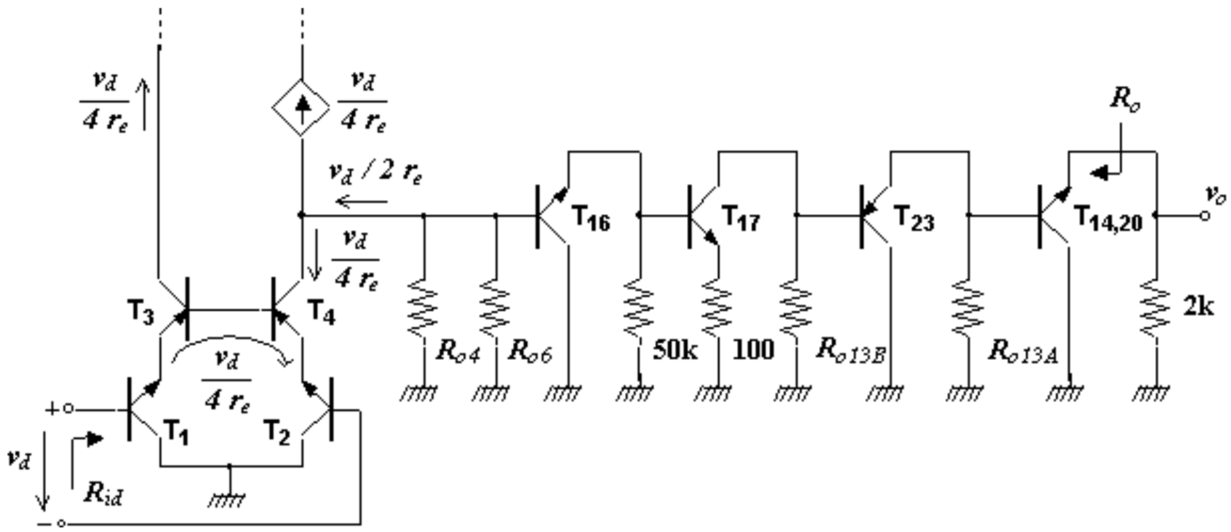


fig. 68 – Small signal equivalent circuit of the mA741 OpAmp

Let's also remark that the follower pair is represented by a CC configuration in which the transistor labelled $T_{14,20}$ represents the corresponding set of transistors, which is a fairly accurate approximation.

However, the follower pair has to cope with large signals and therefore its gain varies along the cycle. Moreover the fact that one of the transistors is an *npn* while the other is a *pnp*, is a reason for asymmetry. Let's analyse how much the gain may vary:

$$A_{14,20} = \frac{2k \,//\, r_o}{r_e + 2k \,//\, r_o}$$

If we have I_C = 5 mA, then r_{o14} = 25 kW, r_{o20} = 10 kW and r_e = 5 W, for both transistors, we get

$A_{14} = 0.997$ and $A_{20} = 0.997$

Whilst for I_C = 150 mA, with r_{o14} = 833 kW, r_{o20} = 333 kW and r_e = 167 W, for both transistors, the result will be

$A_{14} = 0.923$ and $A_{20} = 0.923$

As we can see, taking $A_{14,20}$ @ 1 is still a good approximation.

T_{23} is an emitter follower that responds only to small signals, but with a varying load. The load may vary as follows:

R_{i20} = 85 kW - T_{20} having a collector current I_C = 5 mA

and

R_{i14} = 435 kW - T_{14} with I_C = 150 mA.

As $R_{o13A} = r_{o13A}$ = 278 kW, r_{o23} = 278 kW and r_{e23} = 139 W, we'll have

$$A_{23} = \frac{278k//278k \,//\, R_{i14,20}}{139 + 278k//278k \,//\, R_{i14,20}}$$

Therefore,

$R_{i14,20}$ = 85 kW will result in $A_{23} = 0.997$

while for

$R_{i14,20}$ = 435 kW leads to $A_{23} = 0.999$.

Again A_{23} @ 1 is a good approximation.

The limiting situations are

$$R_{i23} = 51\ (139+139k//85k) = 2.70\ MW$$

and

$$R_{i23} = 51\ (139+139k//435k) = 5.40\ MW$$

Let's take the smallest value that somehow compensates for the unit gain approximation.

For T_{17}, that is a CE with emitter resistance configuration,

$$A_{17} = \frac{R_{o17}//R_{o13B}//R_{i23}}{r_{e17}+100}$$

where $R_{o13B} = r_{o13B} = 90.9$ kW and $r_{e17} = 45$ W.

To compute the resistance R_{o17}, we need the resistance R_{o16} and, to compute this one, R_{o4} and R_{o6}.

To compute R_{o4}, the base node of T_3 and T_4 is considered as a virtual ground. This is only possible once the differential gain is being considered.

So, taking into account that $g_{m4} = 380$ mA/V, $r_{p4} = 132$ kW and $r_{o4} = 5.26$ MW,
fig. 69 shows how, by stepwise circuit transformations, we get:

$$R_{o4} = 5M26+5M13+2k57\ @\ 10.4\ MW$$

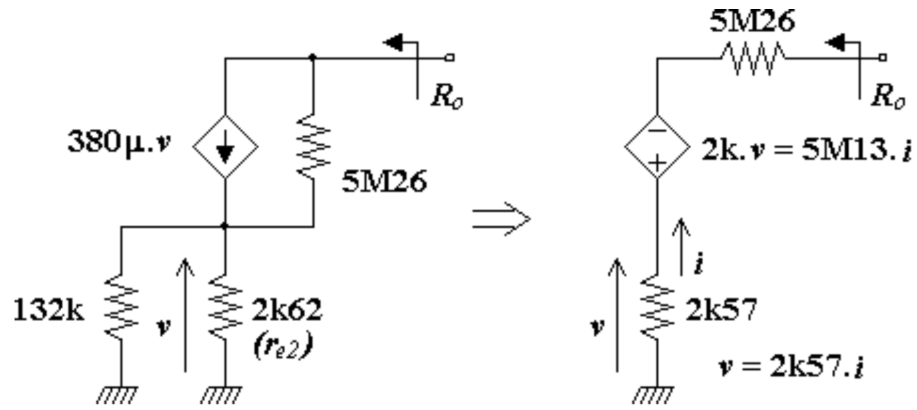


fig. 69 - Evaluation of the output resistance R_{o4}

The value of R_{o6} can again be evaluated in the same way. In fact, the base circuit resistance of T_6, i.e. the resistance of the external circuit is only 19 W (*compute this value as an exercise*), which is very small when compared to r_{p6} . So, since g_{m6} = 380 mA/V, r_{p6} = 526 kW and r_{o6} = 13.2 MW,
it results that

R_{o6} = 18.2 MW.

We can now compute R_{o16}, which is the output resistance of a CC, with a base resistance R_{o4} // R_{o6} and r_{p16} = 309 kW:

$$R_{o16} = \frac{10M4//18M2 + 309k}{200+1} = 32.9\ k\Omega$$

Finally, to compute R_{o17}, taking into account that

g_{m17} = 22 mA/V, r_{p17} = 9.09 kW and r_{o17} = 227 kW, and that the base resistance is é R_{o16} // 50k = 19.9 kW, fig. 70 shows how, again by stepwise circuit transformations, we get:

$$R_{o17} = 100+157k+227k = 384 \text{ kW}$$

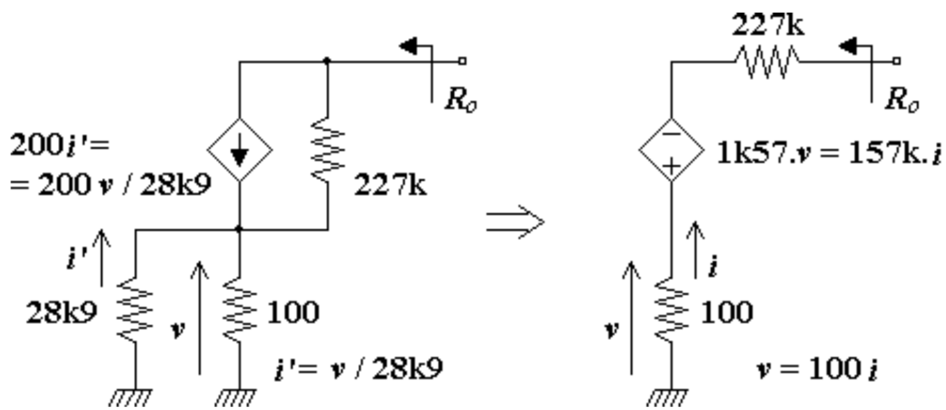


fig. 70 - Evaluation of the output resistance R_{o17}

Therefore A_{17} = -493 V/V.

We also want to get the value of

$$R_{i17} = 9k09+201\,´100 = 29.2 \text{ kW}$$

T_{16} is a CC montage, but as the collector current is very small, will display a high value for r_e. We should make sure that the value doesn't depart very much from unity:

$$A_{16} = \frac{r_{o16} // 50k // R_{i17}}{r_{e16} + \left(r_{o16} // 50k // R_{i17}\right)}$$

where r_{o16} = 7.72 MW and r_{e16} = 1.54 kW,

therefore A_{16} = 0.923.

The input resistance is:

$$R_{i16} = 201\ [1k54+(7M72//50k//29k2)] = 4.00\ \text{MW}$$

Finally, for the differential pair we have:

$$A_1 = -\frac{1}{2r_e}\left(R_{o4} \,//\, R_{o6} \,//\, R_{i16}\right)$$

where r_e = 2.63 kW (approximately common to $T_1 - T_4$).

It results that A_1 = -474 V/V

and finally

$$A_d = -474\ ´\ 0.923\ ´\ (-493) = -216\,000\ \text{V/V}.$$

To compute R_{id} is trivial. Reporting to fig. 68, we can see that

$$R_{id} = 4\ (b_N + 1)\ r_e = 2.1\ \text{MW}.$$

On the other hand, computing R_o, i.e., the output resistance of the complementary symmetry follower pair, can only be obtained as an average value. In fact, as the complementary pair works with large signals the output resistance will depend upon which transistor is conducting as well as upon its current.

If T_{20} is supplying the current

$$R_o = r_{e20} + \frac{R_{o23} // (r_{o18} + r_{o13A})}{\beta_{20} + 1} + 27$$

where $$R_{o23} = r_{e23} + \frac{R_{o17} // r_{o13B}}{\beta_{23} + 1} = 1.73\,k\Omega$$

As r_{o18} is very small compared to r_{o13A} (278 kW), we will have

$$R_o = r_{e20} + 34 + 27$$

The value of r_{e20} depends critically on the current.

For $I_C = 150$ mA $r_e = 167$ W

while for $I_C = 5$ mA $r_e = 5$ W, as seen above.

Therefore, the value can vary between 66 and 228 W. The data sheets specify the value 75 W.